NEW PASSIVATION METHODS FOR GaAs

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NEW PASSIVATION METHODS FOR GaAs

FINAL TECHNICAL REPORT

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Abstract

The fabrication of high-quality oxides on GaAs with good electrical interface properties was investigated. Several primary and subsidiary approaches were explored. The best results were obtained with a new anodization scheme based on an aqueous solution of tartaric or citric acid with glycol, and a subsequent annealing at 250°C. This scheme is suitable for both GaAs and AlGaAs. In view of increased corrosion resistance of the resulting oxides if some amount of Al is included, and in view of an optimization of interface lattice matching, semi-insulating GaAlAs was grown by sliding-boat liquid-phase epitaxy prior to anodization. A new method of depositing pure Al_2O_3 by slow evaporation of Al through an O_2 atmosphere of 5×10^{-4} torr also gave encouraging results which could be understood by the fact that this method is akin to that of molecular-beam epitaxy.

The best electrical interface properties obtained (interface state density about 10^{11} cm^{-2} $(eV)^{-1}$, vanishing capacitance hysteresis versus bias voltage, no frequency dispersion of capacitance etc.) make the results very useful for anti-corrosion passivation of optical devices and for MOS device applications.

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CHAPTER 1

INTRODUCTION

Whereas the passivation of Si is well developed, there are serious difficulties associated with surface passivation of GaAs and other compound semiconductors. These are primarily caused by the high vapour pressure of one of the components such as As so that it is impossible to apply easily similarly high temperatures as usually done for the production of SiO_2. Non-native oxides, which can be deposited at lower temperatures, exhibit poor adhesion, high interface-state densities and increased lateral diffusion of impurities along the semiconductor-oxide interface which is particularly serious in connection with diffusion masking applications.

We felt that a promising exception for GaAs would be a slow deposition of Al_2O_3 together with some Al, particularly at the beginning of the deposition process. Al forms with GaAs a ternary compound with a lattice constant which is very close to that of GaAs. Several schemes were attempted such as evaporation of Al_2O_3 from a W boat at very high temperatures* and electron-beam sputtering without any useful results. However, one of these exploratory efforts gave encouraging results which lead us to embark on a more systematic study of this method. This was slow evaporation of Al through O_2 at a pressure of $5 \cdot 10^{-4}$ torr - a method which is rather related to that of molecular-beam epitaxy. These studies were then performed by R. Singh** and resulted in MOS capacitors with an already useful reduction in interface state densities. This work is being continued by a new comer to our laboratories, A. El-Safti.

Another new approach which was pursued by H. Hasegawa*** is to try to passivate the semiconductor with an insulating

*These early experiments were undertaken here primarily by our colleague J. T. Kennair.

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crystalline structure with a perfect lattice match to the semiconductor rather than the usual scheme of growing a non-crystalline amorphous structure on the semiconductor, in order to obtain, in particular, very good interface properties with low slow and fast state densities. Detailed considerations led to the composite scheme of (1) growth of a semi-insulating GaAlAs layer and (2) partial oxidation of the grown layer by an anodization technique.

However, a series of efforts showed that it is not possible to produce semi-insulating liquid epitaxy layers with Cr doping, as all the layers produced turned out to be not only semiconducting (without any intentional doping, our liquid epitaxy system gives semiconducting GaAs with $n \approx 10^{15}$ cm^{-3}), but highly conducting. This is an indication that Cr could probably then be incorporated as a shallow donor impurity. On the other hand, sufficiently high resistivities were generated with Fe doping. As a by-product, an S-type instability was found with structures made with metal-semi-insulating GaAlAs - n^+ GaAs sandwiches.

An extensive effort was also made to find a suitable anodizing agent of the GaAlAs layer in connection with the proposed composite approach.

In the light of our previous experience, and taking into account all the results reported by other laboratories, including the results reported by B. Schwartz and co-workers[1] on anodization in H_2O_2, we were able to develop, on the basis of various ideas we had, an electrolyte based on an aqueous solution of tartaric or citric acid. By adding a large amount of glycol to this solution, the resulting oxides of GaAlAs became layers of high quality.

More importantly, we have found that also the new electrolyte can produce the native oxide of GaAs with superior dielectric properties. Therefore, detailed growth data of such an oxide has been established..

An automatic C-V measurement system has been

developed by K.E. Forward* and extensive C-V studies of MOS capacitors, made with such a native oxide, have been carried out including annealing effect.

When the oxide layers, produced by our new electrolyte, were annealed at about 300°C, an impressive improvement of the electrical interface properties was obtained, namely an interface state density of about $10^{11}cm^{-2}(eV)^{-1}$, a disappearance of the low-frequency dispersion of the accumulated capacitance previously always observed, and a large reduction of the capacitance bias voltage hysteresis, i.e. a removal of the majority of probable traps in the oxide near the interface. These results are indeed very promising so we decided to fabricate a GaAs MOS transistor in order to measure the surface mobility and other properties of such devices which should have important logic - circuit applications because of such properties as high carrier velocities and mobilities and short excess-carrier life times due to direct-gap transitions of GaAs. This has also been undertaken so far primarily by K.E. Forward and H. Hasegawa. They have recently been joined by a new postgraduate student, B. Bayraktaroglu, who has also looked into the possibility of producing a GaAs CCD in order to study surface properties.

It has also been found that our native oxide of GaAs has poor chemical and thermal stabilities as compared with SiO_2. Therefore, various efforts have been initiated to improve these properties without losing the favourable interface properties.

It was established that Al could be oxidised by our new anodization process. Al_2O_3 is resistant to most etchants and produces therefore a layer of improved long-time stability. Even small traces of Al_2O_3 in native oxide of GaAs improves

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*On leave from the Department of Electrical Engineering, Monash University, Victoria, Australia.

the etch-resistance of the oxide layer. We therefore evaporated Aℓ first onto GaAs and then anodized the whole Aℓ and some part of the GaAs underneath it. The oxide layers thus formed were indeed very stable.

In order to incorporate Aℓ with a uniform level into the oxide, a layer of GaAℓAs was grown by liquid-phase epitaxy on GaAs and subsequently ionized. This epitaxy approach enables one also to a certain extent (depending on the solubility data) to incorporate other elements into the oxide which might have beneficial effects such as an increased thermal and etch-stability of the glassy structure and reduced impurity-diffusion across the oxide layer produced in view of working applications.

Finally, we are continuously searching for other solutions to oxidation of GaAs. An interesting possibility of producing As_2O_3 on the (111) As surface of GaAs by concentrated HNO_3 was studied by B. Weiss.

This report describes therefore the results of evaporation through O_2 gas in Chapter 2, the liquid-epitaxy work on GaAℓAs in Chapter 3, the new-electrolyte data and C-V data of MOS capacitators in Chapter 4, the electronic circuit developments undertaken for a speedy assessment of the electrical interface properties in Chapter 5. Other miscellaneous efforts for oxidation which have been tried are given in Chapter 6, which includes the use of a spin-on SiO_2 film, an anodized $Aℓ_2O_3$ film, an electron-gun deposited $Aℓ_2O_3$ film, native oxide of GaAs produced by a NaOCℓ solution, semi-insulating GaAs and GaAℓAs produced by proton bombardment and an As_2O_3 layer from a HNO_3 solution. Finally, the work undertaken so far on MOSFET and CCD structures is presented in Chapter 7. As appendices, we give the circuit detail of the C-V data and list of papers submitted for publication.

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CHAPTER 2

DEPOSITION OF Al_2O_3 on GaAs BY EVAPORATION OF Al THROUGH O_2 GAS

(R. Singh)

2.1 INTRODUCTION

It is described here how Al_2O_3 is deposited on GaAs by a slow evaporation through a low pressure of oxygen. This method is similar to that of molecular-beam epitaxy (1). A measurement of the interface state density shows that this is reduced, as compared to the values obtained with other common methods of covering GaAs by an oxide. It can therefore be expected that further reductions can be achieved by exploring this method more deeply.

Our interface state density is determined across part of the energy gap near the flatband condition. Results indicate that the density peaks near the conduction band edge in a similar manner as in Si, but that the density function does not vary as strongly with energy as found for Si.

2.2 Al_2O_3 DEPOSITION

We have manufactured Al_2O_3 on GaAs slices (Orientation 100) by evaporation of Al through a low O_2 atmosphere.

The etched and cleaned epitaxial GaAs (n-n^+) sample was first supplied with a good ohmic contact on the n^+ substrate face, by evaporating In-Ge-Ag films and alloying in a hydrogen atmosphere at 620°C for 1 min. The ohmic contact thus formed, was covered with a layer of photoresist to protect it during etching of the epitaxial layer for the deposition of Al_2O_3. The etch solution used was $NH_4OH:H_2O_2:H_2O$ of the ratios 1 : 4 : 20. The slice was then mounted in a vacuum evaporator. An Alumina coated molybdenum boat was charged with a small quantity of 99.999% pure Aluminium. When the vacuum pressure in the chamber was reduced to better than 10^{-6} torr, the boat temperature was slowly raised to about 1100°C and Aluminium was evaporated for 5 minutes against closed shutter. This step is necessary in order (1) to remove any surface contamination on

the Aluminium by first evaporating against a shutter for a short time and then (2) to cover all freely exposed elements present in the chamber with an Aluminium film which will avoid oxidation and evaporation of any material other than Aluminium. Setting the temperature then just below evaporation, oxygen was admitted into the chamber such that the equilibrium pressure of the outgoing gases and incoming oxygen is 5×10^{-4} torr. Five minutes later when the Aluminium vapours were fully saturated with oxygen, the shutter was opened and the epitaxial layer was exposed to a slow deposition of Aluminium Oxide. The distance between the source and the sample was more than the mean free path of the molecules at this pressure.

Thus, oxygen present in the chamber is permitted to react with Aluminium at the molten surface, in the vapour phase and at the epitaxial layer surface. This feature ensures that the layer in immediate contact with the GaAs surface is Al_2O_3 and of the same quality as the top layer. Moreover, it results in a higher yield than that of other methods.

When the desired thickness of around 1200Å of Al_2O_3 is grown the shutter is closed and the heater supply switched off. The sample was then allowed to cool down, exposed to air and placed in an oven at 150°C for 3 hours to anneal the layer and to complete oxidation of any not fully oxidized Aluminium near the surface. Subsequently a metal electrode as a field plate is deposited by evaporating Aluminium under a good vacuum.

2.3 ELECTRICAL MEASUREMENTS OF THE METAL - OXIDE - GaAs STRUCTURE

It is important to establish the charge state density at the semiconductor - oxide interface as a function of the energy across the energy gap, and the relevant charge-capture time constant T of these states. This can be obtained most conveniently by measuring the rf conductance as a function of angular frequency ω, from which the equivalent interface-state conductance G_p can be derived (2). The function $G_p/\omega = f(\omega)$ peaks at $\omega T = 1$, where its value gives also directly the interface state density N_{SS}. Unfortunately, this convenient method is only strictly possible if N_{SS} is not a continuous function of energy but is present at a discrete energy level

only. The more accurate method for a continuous N_{ss} function involves a rather sophisticated evaluation procedure. However, it becomes doubtful whether the more involved procedure is justified at this stage of order-of-magnitude investigations of GaAs oxides, because it is quite possible that these structures show very different phenomena from those of Si - SiO_2 and that a different equivalent circuit to that given by Nicollian et al (4) is valid. Therefore it was decided to undertake the conductance evaluation by assuming a quasi-single-state behaviour. A comparison of N_{ss} for Si O_2 on GaAs gave the same value as obtained by Adams et al (3) so that the error produced by our assumption seems to be negligible. Unfortunately, it is only possible to obtain peaks of G_p/ω with our Boonton Electronics Direct Capacitance Bridge for conditions when the Fermi level is near to the conduction band with our n-type material, as the value of T is then sufficiently short for the peaks to occur above the minimum frequency of operation for our bridge, namely 5 kHz. Several types of GaAs slices were used and tested and the results were basically the same. The data of the sample where results are presented below is as follows:-

Gas-epitaxy 0.77Ωcm layer of 6μ thickness and of mobility 7000 cm^2 /Vsec on n+ substrate, orientation (100) : thickness of Al_2O_3 layer : 1200Å as determined by profile measurement with Dektak profile plotter after a slow evaporation process of 30 min. with a distance of 18 cm between evaporation source and sample. The insulator capacitance C_i was determined by fabricating an Al - Al_2O_3 - Al sandwich on a glass substrate by a separate evaporation process with the same parameters as used for the oxide on GaAs, and it was found that $C_i = 15_pF$. The interface density obtained and the charge filling time T are shown in Fig. 2.1.

A measurement of the device capacitance with bias voltage V_B shows that after the application of a positive bias voltage of about 2 Volt, the capacitance curve is shifted upwards by typically 0.8 pF. It can be assumed that this is caused by some traps filled in the insulator by the application of a positive bias voltage. It is found that this shift cannot be removed by the application of a negative V_B up to at

least - 3 volt, and that it is maintained over many days. By correcting the measured capacitance increase due to this trapped insulator charge and by the removal of the series connected insulator capacitance C_i, the space charge layer capacitance C_D is found as a function of V_B. This is shown in Fig. 2.2. This information can be used to find the approximate values of voltage V_s at the semiconductor surface and corresponding scales have been introduced on Figures 2.1 and 2.2. The results of Fig.2.2 can be used to obtain the flat-band voltage V_{FB} by taking the flat-band capacitance of our material, which is C_{FB} = 59.9pF where we used the relative permeability for GaAs, ε_R=12. This gives a flat-band voltage V_{FB} = +0.5 volt, which determines the value of the negative fixed charge near the semiconductor surface inside the insulator, namely 6 x 10^{10} cm^{-2}. The above described capacitance - curve shift of 0.8pF after the application of a positive bias voltage can be used to determine the density of slow traps and it is found that they are also about 6 x 10^{10} cm^{-2}.

In an attempt to obtain an estimate of N_{ss} for V_B < 0.7 Volt, when the conductance peaks occurred at frequencies below the measurement range of our Boonton Bridge, we measured carefully capacitance versus frequency for various bias voltages. After removing the contribution of the series-connected C_i, we obtained the capacitance C_p. If the model of Nicollian and Goetzberger (4) is correct for our oxide structure, C_p would have to satisfy a given frequency dependance. Unfortunately, our experimental findings do not fit the required dependance and it seems likely that different types of additional states with different charging times have to be taken into account which could be relatively fast traps inside the oxide. The corresponding time constants could be expected to be higher than those of the interface states because they can only be filled by a tunnelling process with reduced probability. It appears from the experimental data that the equivalent circuit does not have a series RC branch connected in parallel to C_D as proposed by Nicollian et al (4), but in parallel to C_s. This could indicate that the traps can only be filled via a two-step process involving an intermediate transfer first into the interface states.

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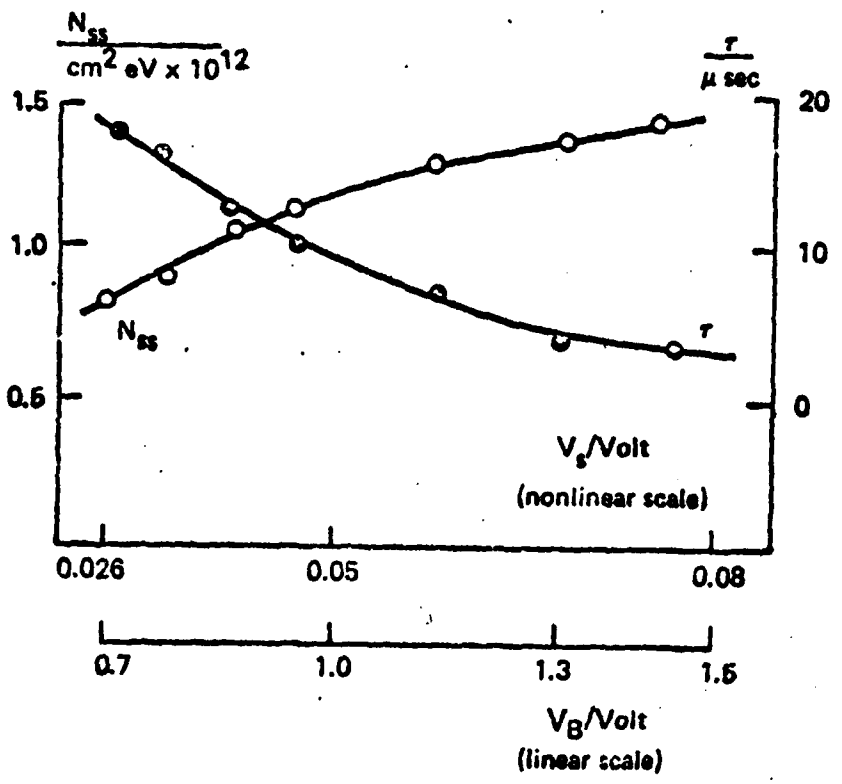
FIGURE CAPTIONS

2.1 Interface state density N_{SS} and charge capture time T versus bias voltage V_B applied to the MOS sandwich applied and approximate semiconductor-surface potential V_S for Al_2O_3 deposited by evaporation of Al through O_2.

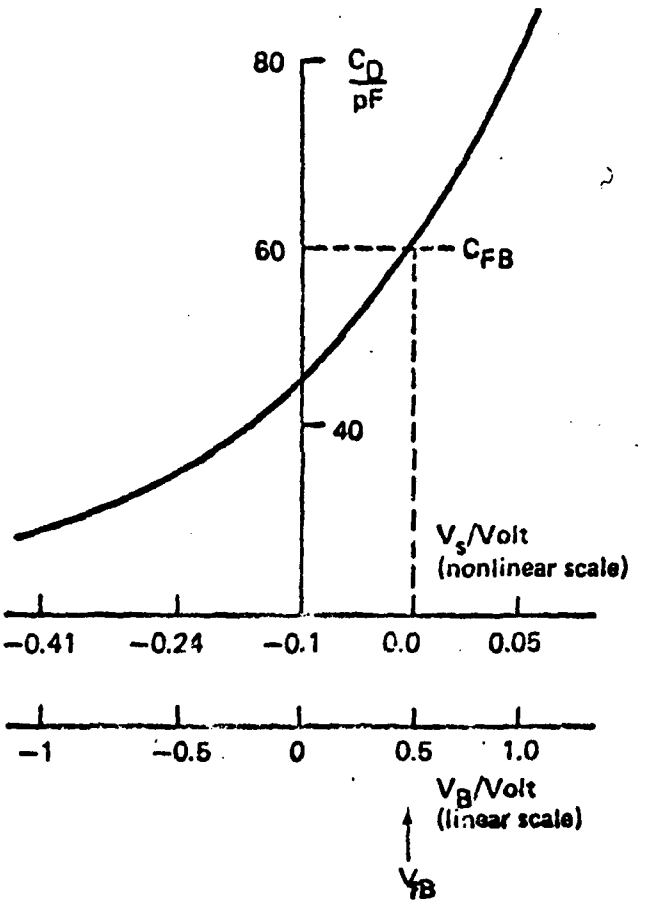
2.2 Space-charge capacitance C_D versus V_B and V_S for Al_2O_3 sandwich of Fig. 2.1.

Fig. 2.1



Interface state density N_{SS} and charge capture time τ versus bias voltage V_B applied to the MOS sandwich and approximate semiconductor-surface potential V_S for Al_2O_3 deposited by evaporation of Al through O_2.

Fig. 2.2



Space-charge capacitance C_D versus V_B and V_S for Al_2O_2 sandwich of Fig. 2.1.

CHAPTER 3

PASSIVATION SCHEME UTILIZING GaAlAs LPE LAYER

(H. Hasegawa)

3.1 DESCRIPTION OF PASSIVATION SCHEME USING LPE GROWTH

It has been well recognised now that one of the main purposes to provide a passivating layer on a semiconductor surface is to "electronically" passivate the surface, i.e. to provide a nearly ideal transition from the active semiconducting region to a passive insulating region without introducing additional electronically active states at the interface which will deteriorate operation and stability of the device. The exact physical origins of these interface states have not been clarified yet even in the case of the $Si-SiO_2$ system, but it is generally accepted that these states are associated with some types of structural defects at the interface (1)(2). This fact seems to suggest that, if one can grow an insulating crystalline material in an epitaxial single-crystal form with a complete lattice match to the semiconductor, it will provide an excellent passivation layer. Such a scheme is an opposite extreme form of passivation as compared with the usual style where a crystalline structure is transformed to an amorphous glassy structure.

Clearly, the success of such a scheme depends on the availability of the insulating crystal with a good lattice match to the semiconductor.

Fortunately the intrinsic carrier concentration of GaAs and related ternary compounds is low at temperatures of usual device operation due to wide energy gaps, so that semi-insulating crystals could be grown either in the usual deep-level compensated form or even "undoped" form, epitaxially on GaAs surface with a good lattice match.

On the other hand one can not expect the excellent dielectric breakdown properties usually found with good insulating oxide materials. The

current conduction and electrical breakdown phenomena in semi-insulating GaAs are known to be well explained, at least qualitatively, by the space-change-limited current and double injection theories of Lampert and others (3) (4) (5). According to the experimental results the maximum resistivity so far obtained is of the order of 10^8 ohm-cm and the breakdown voltages reported in the literature (6) vary from 15V to 150V for bulk semi-insulating materials with the thickness of 150μm, depending on whether the material is undoped, oxygen doped or chromium doped, and on the type of contacts used. If one also takes into account that the so-called trap-filled-limit-voltage, which gives a rough measure for the breakdown voltage of semi-insulating materials under carrier injection, varies in proportion to the square of the thickness (3), the breakdown voltage of the semi-insulating layer with several micron meter thickness will be estimated to be only few volts at best. This means one needs the additional formation of an insulating layer by suitable means on the free surface to prevent carrier injection from outside and to improve the overall dielectric properties. Although various oxide or nitride deposition schemes could be employed for such a purpose because requirements for interface properties are not so severe there, a somewhat different scheme has been pursued in the work reported here.

It is a two-step passivation scheme utilizing the liquid phase epitaxial growth of GaAlAs layer, which consists of

(1) the formation of a thin semi-insulating GaAlAs layer on GaAs by LPE techniques

and

(2) the subsequent partial oxidation of the LPE layer by anodization techniques.

The reasons why GaAlAs is particularly chosen are as follows: (1) GaAlAs has a close lattice match to GaAs; (2) GaAlAs has a wider energy band-gap and should form a heterojunction barrier to the carriers in GaAs: (3) a more chemically and thermally stable native oxide could be formed on GaAlAs than on GaAs, because of the inclusion of Al atoms which have high oxygen affinity.

The epitaxial growth of a GaAlAs layer on GaAs can be easily done by liquid-phase-epitaxy, while vapour-phase growth of this material (7) still seems to remain at its early stage. A horizontal sliding LPE system developed at this laboratory by A. Colquhoun has been used for the present work, which is basically similar to that described by Panish et al (8) for the fabrication of double-heterojunction laser diodes.

Unfortunately the work reported is still incomplete in the sense that it has not yet reached the stage where a full and final assessment of the proposed passivation structure is possible, although each of the steps leading to the structure has now been well established. This is partly because of the difficulty encountered in growing chromium-doped semi-insulating GaAlAs layers by the LPE technique, which had not been foreseen. Another reason is that the extensive effort to find a suitable electrolyte for anodization of GaAlAs layers has led to the discovery of a new electrolyte which has been also found to give excellent results on GaAs and which has led to the work reported in Chapter 4.

The next section describes the details of the growth of GaAlAs semi-insulating LPE layers and an S-type instability observed in Fe-doped layers. The details of the anodization process will be given in Chapter 4 in connection with the native oxidation of GaAs. One of the main differences between native oxides of GaAs and GaAlAs is that the latter has a higher chemical stability as verified by various etching experiments. This is also consistent with the result reported by Schwartz et al (9) where the native oxide of GaAlAs layers was prepared by boiling in an aqueous H_2O_2 solution.

Although the work concerning anodic native oxide gives a great hope to passivate GaAs in a similar simple manner to Si, which certainly makes the composite approach described here less attractive, we still believe that it is worthwhile to pursue it further in future, not only because passivation by a crystalline structure is conceptually interesting, but more importantly because it would give a structure which is more stable chemically and thermally than the structure based on the native oxide.

3.2 EPITAXIAL GROWTH OF SEMI-INSULATING GaAlAs LAYER BY LPE TECHNIQUE.

A typical horizontal sliding-boat liquid-phase-epitaxy system as shown in Figure 3.1 with a Pd-diffused hydrogen flow was used for the experiment. A high-purity high-density carbon slider was designed and constructed for the purpose.

n-type GaAs bulk materials (Si-doped) with (100) orientation were used as the substrates for the growth. The temperature starting the growth was in the range of 780~830°C and the cooling rate of typically 1°C/min. was employed. A high-precision PID temperature control system (Eurotherm) was used to produce the controlled temperature variation.

The substrate size is 3 x 6 mm^2 and the growth was done from a Ga-rich melt which is typically 600~1000 mg in the total weight. To prepare the melt a suitable amount of undoped polycrystalline GaAs and a suitable amount of the deep level dopant were put into Ga solution and heated up and kept in a H_2 flow for several hours at a temperature which is higher than the actual growth temperature. This is to ensure the complete dissolution. Then, after cooling down, a suitable amount of Al is added to the melt and the substrate is loaded to the slider to start the actual growth.

A careful cleaning procedure was applied to the substrate before putting it into the growth system which includes a series of ultrasonic cleaning in various organic solvents, a "Soxlet" recycling cleaning in isopropyl alcohol and boiling in HCl solution.

To establish the basic performances of the growth system various LPE layers were produced without doping the melt with the "deep-level" impurities. $Ga_{1-x}Al_xAs$ LPE layers with x being from 0 to 0.3 and with a thickness ranging from 1 to 30 μm were grown with reasonably good surface appearances. The value of x was determined by the X-ray microprobe analysis and the thickness of the epitaxial layer was measured by delineating the boundary between the epi-layer and substrate with a potassium ferricyanide etchant. It is well known that even a small lattice

mismatch of a few fraction of a percent can give rise to the heterojunction interface state density as high as 10^{12} cm^{-2}. Therefore x was restricted to the above range of 0 to 0.3 by taking the simple theoretical expression for the dangling bond density as the measure for such states and by limiting this value well below $10^{11} cm^{-2}$ (10). The conduction type of the "undoped" GaAlAs LPE layers has been found always n-type with the carrier concentration of less than 5×10^{15} cm^{-3}. The carrier concentration was determined by the C-V measurements on the reverse-biased Schottky diode with a Ag or Al electrode using a Boonton Bridge.

As the dopants to produce semi-insulating GaAlAs by the deep-level compensation mechanism, various dopants have been tried. These include chromium, chromium oxide (CrO_3, Cr_2O_3), gallium oxide (Ga_2O_3) and iron, and, as described in what follows, only iron has been found to produce highly resistive layers, while all the other dopants gave rise to highly conducting layers in the cases of both GaAs and GaAlAs. In order to prevent mixing up of different dopants, a thorough cleaning procedure was applied to both of the quartz furnace tube and slider after the experiments on each dopant, including slight etching by HF solution for the tube and cleaning with aqua regia, prolonged boiling in water, heating in vacuum (10^{-6} torr) and gettering impurities by undoped pure Ga liquid.

Chromium is added to the Ga-melt in the form of powder. According to the literature (11) chromium is attached by Ga and dissolves into the melt above 600°C. The concentration of the chromium in the melt was varied from 1% up to the maxiumm of 10% by weight but within this range the grown layers of GaAs and $Ga_{1-x}Al_xAs$ ($x \leq 0.3$) were found to be all n-type and highly conducting with the carrier concentration being in the range of 10^{16} - 10^{17} cm^{-3}. Although chromium is known to be the best dopant for the growth of semi-insulating GaAs by the Czochralski method, the present result indicates that this is no longer true for the epitaxial growth of GaAs and GaAlAs by the LPE technique. There could be several possible explanations for this different behaviour. For instance

(1) the segregation coefficient, k, of Cr is too small in the case of LPE or (2) the solid-solubility of Cr is too small, either of which can lead to the situation of an insufficient number of Cr atoms to compensate the "residual" donors of about 5×10^{15} cm^{-3}. However if (1) is the case, the effective segregation coefficient of Cr should be at least 5×10^{-6} to explain the experimental result. This seems too small as compared with the published data of the segregation coefficient of about 5×10^{-4} at the stoichiometric condition (11) (12) (13), even if one takes account of the differences of the growth conditions. In this sense, case (2) is more probable because the solid solubility of heavy-metal deep-level impurities in both Si and GaAs can take quite commonly the value in the range of 10^{15} cm^{-3} at the temperatures of 600 - 800°C. In fact this seems to be the case for the vapor-phase epitaxial growth of Cr-doped semi-insulating GaAs using chromyl chloride reported by Mizuno et al (14), where successful growth was done only when the donor concentration of the layer is below 5×10^{15} cm^{-3}. However, for the present case, neither of above (1) and (2) can explain the high carrier concentrations consistently observed in the growth GaAs and GaAlAs layers.

Other possible behaviours are as follows. Although a sufficient number of Cr atoms are present in the grown layer, they are no longer making the usual deep acceptors but acting either (3) as electronically inactive impurities or (4) actively as shallow donors. The case (3) is known to be quite common in Czochralski bulk materials where a certain fraction of Cr atoms are always found to stay in the crystal being electronically inactive (11) (15). The same type of inactivity has been also reported in the case of diffused chromium (16). As for the case (4), E. Andre et al (17) has reported that Cr acts like a shallow donor in the LPE GaAs, although the segregation data of $k \sim 10^{-5}$ obtained by them seems too small to explain the present case.

Apparently the present result seems best explained by the case (4) of the above with the effective segregation coefficient of the order of 10^{-4}, although the other possibilities cannot still be completely ruled out.

Obviously the behaviour of chromium in GaAs and GaAlAs is very complicated and future work is necessary to explain all the experimental facts in a self-consistent manner. To clarify the actual position taken by the chromium atom in the crystal lattice seems particularly important for such a work. For example, it seems not too unrealistic to assume that the usual deep acceptor level is associated with the chromium atom substitutionally put into the Ga-site which would become less possible in the Ga-rich situation of the LPE growth.

The doping of chromium oxide was also done in the form of powder. Two types of oxide, i.e. CrO_3 and Cr_2O_3 were tried and both failed to produce semi-insulating layers. The reason of trying chromium oxide was based on the experimental observation (18) that most of the good Cr-doped semi-insulating GaAs tends to contain oxygen atoms whose number is nearly equal to that of Cr-atoms which seemed to suggest a possible presence of a certain type of Cr-O complex. The present result obviously cannot rule out such a possibility because both the extremely unstable and volatile nature of CrO_3 and the extremely stable nature of Cr_2O_3 could equally become the cause for insufficient doping into the melt. Doping by up to 10 wt. % into the melt has been tried and resulted in n-type conduction with the carrier concentration in the low 10^{16} region in both cases.

Iron was doped in the form of wire into the melt in the range of 2-7 wt. % and it has been found that such a doping can give rise to a very highly resistive p-type epitaxial GaAlAs or GaAs layer with the specific resistivity of the order of 10^3-10^4 ohm.cm which is consistent with the double deep-acceptor levels of Fe reported in the literature (19).

The detailed electrical properties of the iron doped LPE layers were studied further by depositing metal contacts and forming M-i-n (metal-semi-insulator-semiconductor) diodes which is an alogous configuration to the MOS structure. Aluminium is used as the contact material. Thickness of i-layer was 10 to 30μm. The current-voltage characteristic of such a diode has been found to show a reproducible S-type negative instability. A typical V-I characteristic is shown in Fig. 3.2. The forward characteristics (defined as the metal

contact positively biased) of the current I shows a linear dependency on applied voltage V at first up to around 1-volt, which is then followed by a half-power sub-linear dependency of $I \propto V^{0.5}$. This persists up to around 10V and after that, a short super-linear portion of approximately $I \alpha V^2$ appears. Subsequently, the diode shows an abrupt jump into a low-voltage high-current state resulting in a current-controlled negative resistance. The typical threshold voltage is 15V to 20V. In the reverse direction (metal contact negative), the linear dependency persists up to higher voltages of around 10V, gradually changing into a super-linear dependency. According to the theory on the pre-breakdown current in semi-insulating materials (20), a sublinear dependency of current on voltage is a characteristic feature of the semiconductor in the "relaxation regime" in which the minority carrier life time is much shorter than the dielectric relaxation time. However, it is not clear at present whether the observed behaviour is caused by this mechanism which does not seem to have been established fully by the experiments (23) or by some other mechanism such as field-dependent trapping.

The mechanism responsible for the negative resistance is most probably the trap-dominated double injection first proposed by Lampert (4), which leads to a filamentary conduction in the post-breakdown region. Such conduction has been observed with GaAs p-i-n diodes with chromium (21) or oxygen doped i-layer (22) (23). The same type of situation would occur in M-i-n diodes if holes are injected from the metal contact, which is highly probable because of a low Schottky barrier height for holes of GaAs cuased by the pinning of the Fermi level (24).

Nearly trap-free space charge limited current conduction which is very similar to that observed in silicon (25) was also observed by reducing the i-layer thickness to 3∿5 μm before depositing metal contacts. Both single and double injection behaviour were observed which is consistent with the above explanation for the S-type instability.

By placing an approximate resistor of 5∿100kΩ in series, the negative resistance diode shows relaxation oscillations whose frequency and waveform can be changed by changing the

resistance and bias point. Maximum frequency for the diodes with the contact area of about $10^{-3}cm^2$ is 10∿20 MHz. A typical oscillation waveform is shown in Figure 3.3(a). A similar oscillation associated with a filamentary conduction has been reported in the case of a GaP p-i-n diode (26). Under certain conditions, relaxation oscillations involve a very fast transient spike as shown in Figure 3.3(b) which is similar to the behaviour of the picosecond pulse generating diode proposed by Yamashita et al (27), although the I-V characteristic including the bias polarity is quite different.

Such a negative resistance effect in M-i-n diodes could have interesting device applications utilizing the stable, reproducible and fairly fast switching and oscillation behaviour, a simple structure and a simple solution of device isolation. However, it does represent a limitation for direct applications to passivation or MOS type devices, as has been mentioned already at the beginning of the previous section. But, since the instability in question is caused by the carrier injection and high field, it should be avoided by employing the composite structure proposed in the previous section. One might still worry about the effect coming from traps in the compensated semiconductor region of such a structure, but it could be made negligible by making the semiconductor region sufficiently thin, taking full advantage of the fine controllability of the anodization process on thickness.

Finally, doping of oxygen was tried in the form of Ga_2O_3. Most of the grown layers showed again n-type high conduction, being consistent with the experimental observation (28) (29) that oxygen behaves like a shallow-donor rather than a deep donor in LPE gallium arsenide. Some of the M-i-n diodes made from oxygen doped GaAs layers also showed a similar negative resistance effect with a smaller threshold voltage of around 4 to 5 V for an i-layer thickness of 5∿10μm. However, this was not reproducible and needs further study.

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FIGURE CAPTIONS

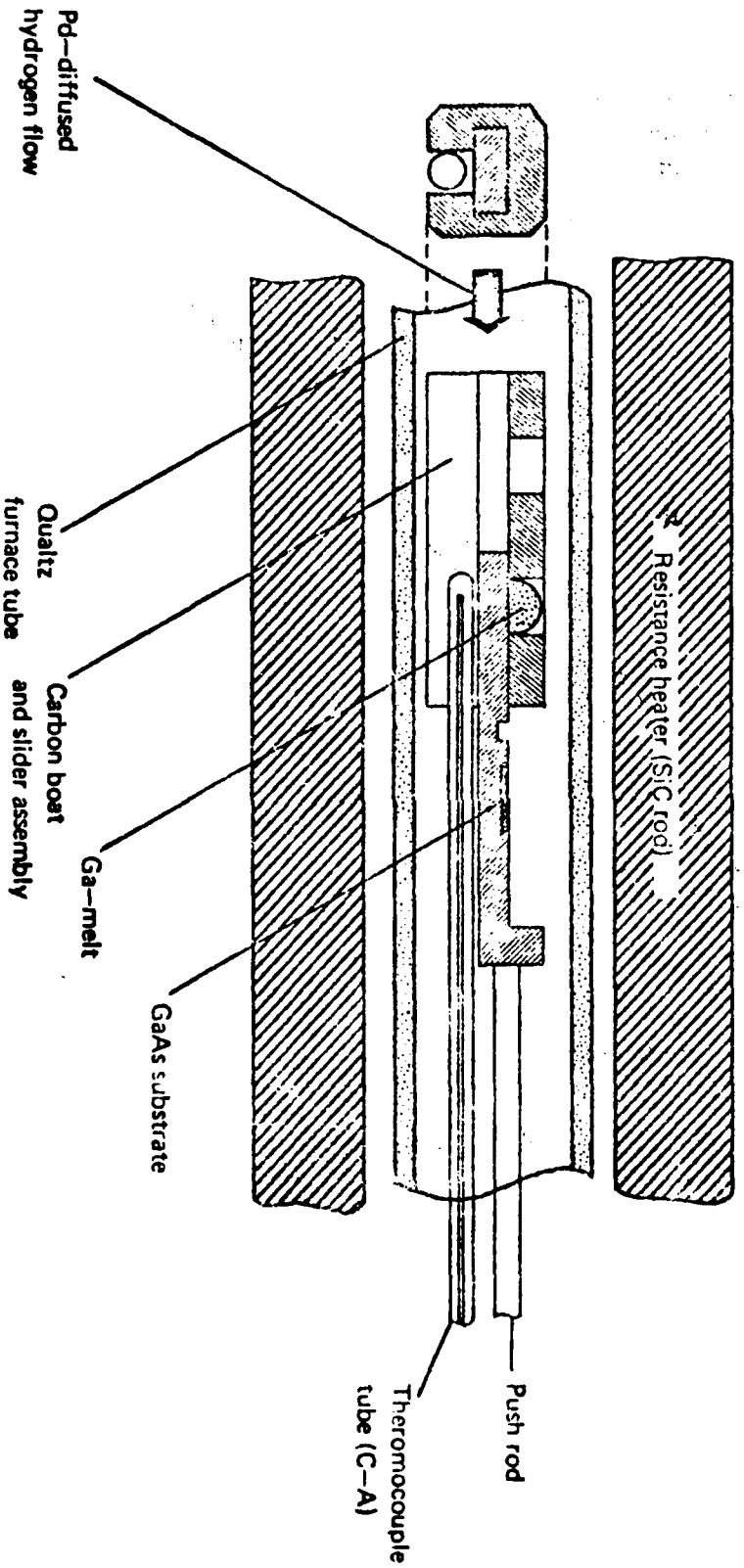
3.1 Schematic diagram of the horizontal sliding-boat LPE system.

3.2 I-V characteristic of a Fe-doped M-i-n diode.

3.3 (a) Oscillation waveform of a Fe-doped M-i-n diode.

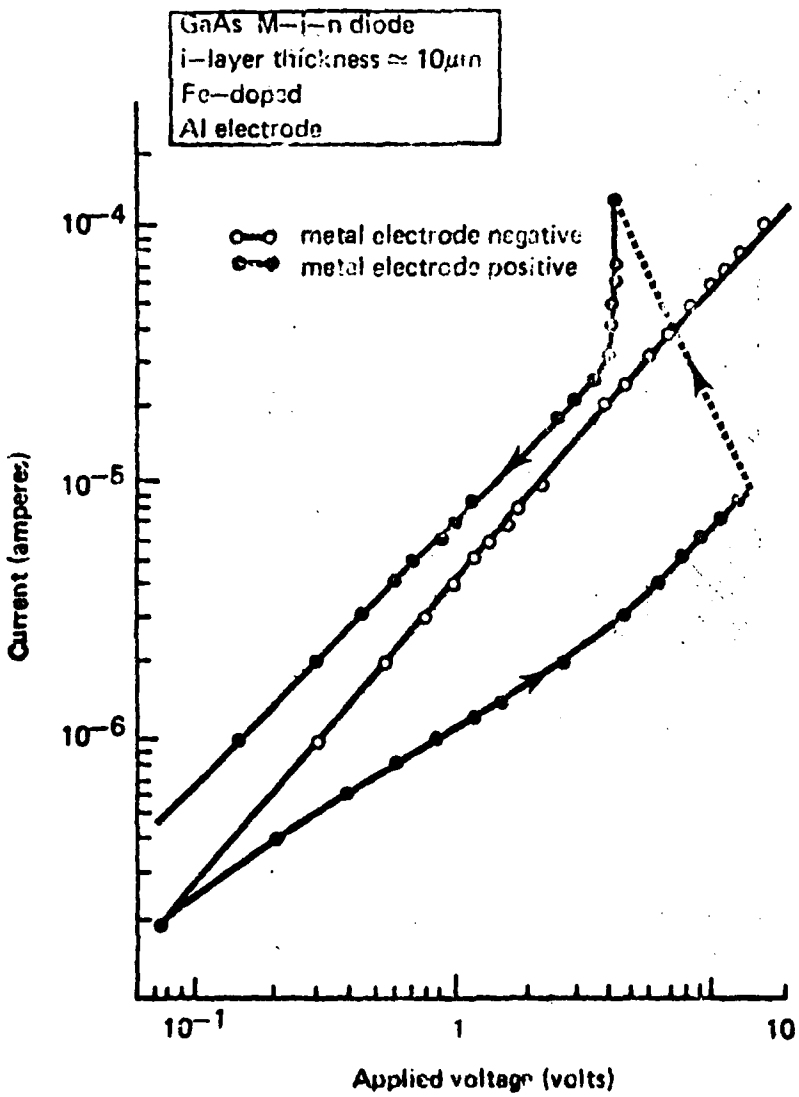
(b) Rel axation oscillation including a fast transient spike.

Fig. 3.1



SCHEMATIC DIAGRAM OF THE HORIZONTAL SLIDING-BOAT LPE SYSTEM

Fig. 3.2



I-V CHARACTERISTIC OF A FE-DOPED M-I-N DIODE

CHAPTER 4

ANODIC OXIDATION OF GaAs

(H. HASEGAWA)

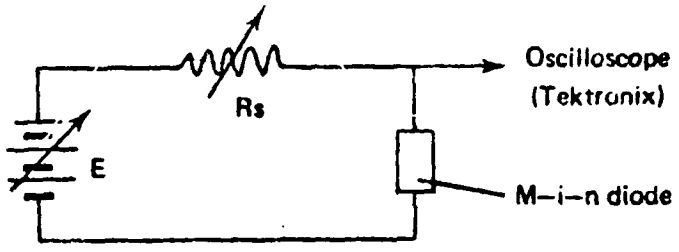
4.1 INTRODUCTION

The simplest and most natural approach to form an insulating layer on a semiconductor surface would be to partially oxidize the semiconductor itself. The impressive success in the Si-SiO_2 system strongly suggests inherent superiorities of such a "native" oxide. However, for this approach of native oxidation to be also useful in the case of GaAs (and other compound semiconductors), the essential question is the availability of a suitable process which can produce a uniform native oxide with reasonably good thermal and chemical stability and a suitable structure i.e. an amorphous glassy structure rather than a polycrystalline structure.

The thermal oxidation which gives the best results in silicon technology is obviously not suitable to the oxidation of GaAs because of the high temperature involved. This high temperature firstly can cause the decomposition of GaAs itself above the so-called decomposition temperature (632°C) due to the high volatility of As atoms and secondly would also violate the thermal stability of the formed native oxide because all known forms of arsenic oxides (As_2O_3, As_2O_5) again decompose or sublime at high temperatures.

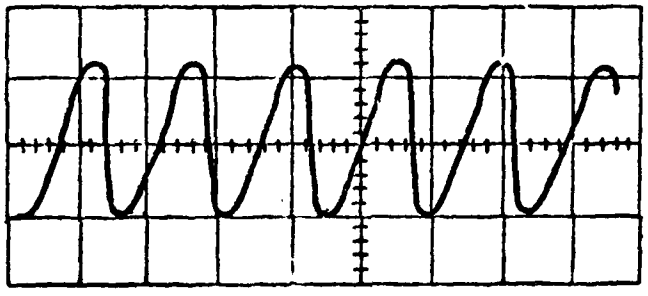
Among the various oxidation processes which could be carried out at relatively low temperatures, such as the accelerated oxidation in high-pressure steam, plasma oxidation (1) etc., the anodic oxidation in an H_2O_2 electrolyte, proposed by Logan et al (2) seems to be the most promising low-temperature process in the sense that it is the only reliable method known so far which can produce a glassy native oxide layer of relatively high resistivity. Although no data has been reported so far concerning its MOS properties except a certain result on the similar oxide on GaP, such an oxide would posses a large potentiality to MOS applications. In addition,

Fig. 3.3



Oscillation waveform of a Fe-doped M-i-n diode

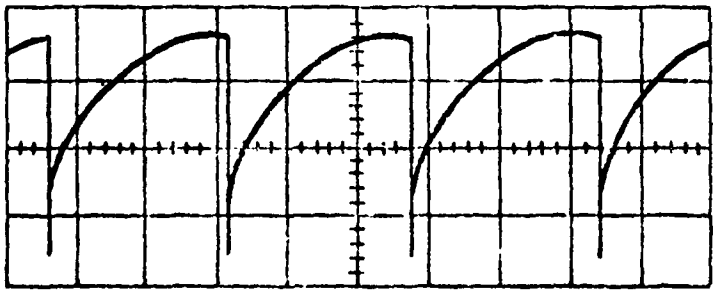
(a)



Horizontal 500 ns/div
Vertical 1 V/div

Relaxation oscillation including a fast transient spike

(b)



Horizontal 2μs/div
Vertical 4V/div

Conditions: large series resistor and near-threshold bias

interesting applications for GaAs device processing have been proposed, which includes not only masks for mesa-etching (2) and diffusion (3) but also an extremely accurate electrochemical etching technique which is particularly useful in the fabrication of GaAs microwave MESFET's (4).

However, from the practical point of view, the following properties of the H_2O_2 electrolyte scheme as described in the literature (2) could provide rather serious difficulties in its practical exploitation.

(1) The process lacks stability against impurities in the electrolyte and the presence of even a few ppm of very common acid like HCl or HNO_3 can turn the oxidation into etching of the semiconductor.

(2) The resulting oxide cannot stand the vacuum deposition of high-melting-point metals such as Au and produces a Schottky contact rather than a high impedance MOS capacitor (Pb has been used so far to make MOS capacitors). This seems to suggest a low-density porous structure of the oxide and could impose a serious limitation on the utility of the oxide.

(3) The pre-breakdown leakage current through the oxide is 10^{-6} to 10^{-5} A/cm^2 which is rather too high (the resistivity is of the order of 10^{11} ohm-cm).

The anodization work reported here has been started naturally to follow this H_2O_2 scheme at first and ran into difficulties because of the above properties (in particular (1)). Extensive efforts to get around these difficulties in turn have resulted in finding a new electrolyte which can solve completely all the above problems and can at the same time provide various additional advantages.

The new electrolyte is a suitable mixture of (1) water, (2) weak carboxilic acid (tartaric or citric acid) and (3) polyhydric alcohol (ethylene glycol or propyrene glycol) and can produce in an extremely stable and reproducible manner a glassy native oxide layer which has the specific resistivity of

10^{14} - 10^{16} ohm cm and the breakdown field strength of 5 x 10^{6} V/cm.

In view of the large potential applications of our native oxide to MOS applications, an extensive study on C-V characteristics has been done and it has been found that annealing of the oxide at a relatively low temperature in hydrogen can improve the interface properties a great deal. The best result shows the density of fast interface states of 1-2x10^{11} $cm^{-2}eV^{-1}$ near the mid-gap with a small capacitance-voltage hysteresis and a small frequency dispersion of capacitance.

The details of the anodic oxidation process is described in section 4.2 and the C-V data will be discussed in section 4.3. Section 4.4 describes briefly a new double-oxide structure which can be produced with the use of the same electrolyte.

4.2 Anodic Oxidation of GaAs using the New Electrolyte

As mentioned in the previous section, the new electrolyte is a suitable mixture of (1) water, (2) weak carboxilic acid and (3) polyhydric alcohol. So far, tartaric and citric acid has been tried as the acid, and ethylene and propylene glycol as the polyhydric alcohol, and each combination of these has been found to work equally well. This suggests that many variations would also be possible for the choice of acid and alcohol.

Practically, the new electrolyte can be conveniently made up by mixing an aqueous solution (3-5%) of the acid with the polyhydric alcohol. The appropriate mixing ratio of tartaric or citric acid solution to glycol has been found to be roughly 1 : 2 to 1 : 4 by volume. Before mixing, the pH of the acid solution can be adjusted by NH_4OH.

Anodization using the buffered acid solution only without mixing with glycol has been found possible also under the conditions of extreme purity and carefully controlled pH value, but it tends to lack reproducibility and to result in films with poor uniformity and poor dielectric properties. The point is that mixing with glycol stabilizes the whole process and ensures

growth of uniform and dense films. It also makes the anodization process less sensitive to the pH value of the acid solution. Glycol has been used previously in the anodization of Si(5) and metals such as Ta and Aℓ(6), (7), but its role seems far more essential in the present case. The reason is perhaps closely related to the solubility of the native oxide of GaAs in aqueous solutions (7) which is a strong function of the pH and becomes large towards acid and base limits. It seems very probable that mixing with a viscosious non-aqueous solute could reduce the overall solubility of the oxide in a drastic manner.

In connection with the solubility of the oxide into aqueous solutions, the natural suggestion one might make would be to use an electrolyte which is completely non-aqueous. In fact, to minimize the water content is the usual practice of anodizing Si(9). Recently, Stehen (10) has tried a new type of non-aqueous electrolyte for GaAs. However, the result so far reported does not look so encouraging as compared with the results reported here, and it seems very possible that an aqueous solution is a more efficient and better anodic oxidant of GaAs than non-aqueous solutions.

Muller et al (11) has proposed recently a different type of non-aqueous electrolyte for GaAs using N-methlacetamide which has a similar thickness-voltage characteristic to H_2O_2 case, but details of the process and oxide properties are not known to make meaningful comparisons.

Figure 4.1 shows the experimental set-up for anodization. Pieces of n- and p-type GaAs with ohmic back contacts (In-Ge-Ag for n-type and In-Ag for p-type), are chemomechanically polished in NaOCl solution, and attached to the capillary tube with a high-quality wax. The initial anodization current is adjusted by a series resistor to a few mA/cm^2. Without this resistor, growth occurs much more rapidly but results in non-uniform films particularly when thick films are grown.

The solid curve in Figure 4.2 is a typical variation of anodization current versus time. Uniform glassy oxide layers with well-defined interference colours are grown within 10-20

minutes at room temperature, up to a thickness of about 7000Å, depending on the voltage applied. The make-up of electrolyte for the case of Fig.4.2is one part of 3% tartaric acid solution with pH adjusted to 6, mixed with four parts of propylene glycol.

The thickness is measured by a Zeiss interference microscope and a Dektak profile plotter. As shown in Figure 4.3 the oxide thickness changes in direct proportion to the voltage applied across the formed oxide, at a rate of 21Å/V for p- and n-type samples with (100) orientations. A similar value is reported in (2). Although the behaviour of current versus time changes with bath parameters, this rate remains barely affected. The amount of GaAs consumed during oxidation is also shown in Figure 4.3. Comparison with the H_2O_2 scheme reveals that more GaAs is consumed in the present case to obtain the same oxide thickness. This could be explained in two alternative ways, i.e. more of GaAs dissolves into the electrolyte in the form of native oxide in the present case, or the present anodization gives denser oxide films. However, other experimental evidences on the present oxide such as that the elctrolyte hardly etch the as-grown oxide, that the as-grown oxide is more impervious against metals in the sense that it can bear the vacuum deposition of high-melting-point metals, and that it has a higher resistivity, a higher breakdown electric field strength and a higher dielectric constant, seem to support the latter alternative.

The as-grown oxides show well-defined and regular occurrence of inference colours. Some of the data is listed in Table 4.1. The approximate value of the refractive index estimated from this is 1.8.

The maximum thickness which can be grown by anodization is limited by the electrical breakdown in the oxide which accompanies sharp spikes in the anodization current and results in a pitty oxide surface. It should be noted that, even on such a pitty surface, most of the surface apart from the pits is uniform and has a regular interference colour corresponding to the same refractive index. This makes a large contrast to the H_2O_2 anodization scheme (2) where oxides of different refractive index start to grow towards the maximum voltage (150~180V) of

anodization which finally leads to a completely granular surface.

The maximum thickness of 7000Å obtained without any electrical breakdown (voltage 350 V) is much larger than the reported value of 3000Å in (2). But, it is still purely an emprical value and could be further increased by optimization of the process. It has been noted that the continuous stirring of the electrolyte becomes very important to obtain thicker films. For a further substantial increase of the film thickness, there are two conflicting ideas which could be tried. One is to cool the electrolyte to increase the breakdown voltage of the oxide as has been successfully done in the case of anodization of Si (12), and the other is to heat the electrolyte to make the ionic transport through the oxide more efficient (13). It requires future work to see which of these approaches works better in the present electrolyte, but such an effort to increase the maximum anodizable thickness seems very important in view of application to the planar technology. Actually, the film thickness of 7000Å seems already to offer a possibility of the dielectric isolation of microwave GaAs FET's where thin epi-layers are commonly used.

As has been pointed out in the previous section, one of the difficulties of the H_2O_2 electrolyte system is that it lacks stability against impurities. For this reason, the process stability of the present system was studied by additionally introducing quite strong traces of various common acids and bases into the electrolyte, and excellent stability was always maintained. For example, the effect of HCl is shown in Figure 4.2. In order not to change the gross pH, the pH of the contaminant solution was adjusted beforehand by NH_4OH. Up to several hundred ppms, no change occurs in the anodization current, and it only starts to become seriously affected from a level of a thousand ppm, when the result is still a fairly uniform oxide layer.

The study of the resulting surface with a scanning electron microscope confirmed that it is smooth and featureless. The oxide has chemical properties similar to those in literature

(2), being soluble in most of the acid and base solutions except conc. HNO_3, but insoluble to the halogen-alcohol echant of GaAs. The dielectric and interface properties were successfully studied on MOS devices formed by vacuum deposition of Au or Al and will be described in the next section.

Though anodization of GaAs has been mainly studied so far, the present electrolyte system appears to possess a large potentiality for applications to other III-V compound semiconductor materials. In fact, the anodization of a $Ga_xAl_{1-x}A_s$ LPE layer ($x \leq 0.3$) has been the starting point of this work as already mentioned in the previous chapter, resulting in a native oxide which is chemically more stable than the native oxide of GaAs.

4.3 Dielectric and Interface Properties of the Anodic Oxide.

Experimental MOS capacitors to study dielectric and interface properties of the anodic oxide were mainly fabricated on surfaces of Zn- doped p- type GaAs bulk materials (Mining Chemical Product Ltd.) with a carrier concentration of $N_A = 1.4 \times 10^{17} cm^{-3}$ and (100) orientation. Ohmic back contacts were provided by vacuum deposition of In and Ag films with a subsequent brief annealing at 600°C in H_2. Surfaces to be anodized were polished chemomechanically in an aqueous solution of sodium hypochlorite. Care was taken to minimize possible contamination by sodium ions and by other sources. After a thorough rinse of the polished surface, nearly 10^{4} Å of GaAs was etched away from the surface by a repeated process of anodic oxidation followed by dissolution of the oxide in an HCl solution. Then, the oxides to be studied were formed in a fresh electrolyte. The composition of the electrolyte was one part of 3% aqueous solution of tartaric acid mixed with two to four parts of propylene glycol. A Pt or Al cathode was used and oxides of 1800-2000Å thick were formed. To form field plates Au or Al dots 400-425 μm diameter were deposited in vacuum through a metal mask. Apart from careful bridge (Boonton, General Radio) and electrometer (Keithly) measurements, of capacitance and leakage current respectively, dynamic measurements and rapid assessments of interface properties are

performed with an automatic C-V plotter which was specifically developed for the purpose and whose details will be given in the next Chapter and Appendix. This C-V plotting system can measure the C-V characteristic for a frequency range from 100Hz to 2.5 MHz with sweep speed ranges of 10mV/s. to 5V/s for the field plate voltage. For all measurements the MOS capacitors are enclosed in an electrically shielded light tight box.

As-grown oxides were found to have a breakdown field strength of 4-5 x 10^6 V/cm, a prebreakdown leakage current density of 10^{-11} to 10^{-9} A/cm^2, and a specific resistivity ranging from 10^{14} to 10^{16} Ωcm. These values are 10^3 - 10^5 times larger than the previous results on native oxides of GaAs (2) and are approaching the quality of thermally grown SiO_2 (14). The relative permitivity measured at 1MHz is 7-8 which is considerably larger than the value of 5.4 reported in (2).

A typical C-V plot of one of our MOS capacitors before annealing is shown in Figure 4.4. It has been shown by previous authors that the properties of the interface between GaAs and various deposited oxides (Si_3N_4 (15)(16), SiO_2 (17), Al_2O_3, - SiO_2 - Al_2O_3 (18) (19) are much more complicated than those of Si - SiO_2 interfaces. The main problems associated with C-V characteristics of such GaAs MOS capacitors are (i) field-induced hysteresis which is observable at room temperature, (ii) large frequency dispersion of the accumulation capacitance at low frequencies, and (iii) a high density of fast interface states (mostly in the range of 10^{12} - 10^{13}cm^{-2}eV^{-1}). The results in Figure 4.4 show that such a complicated behaviour is also present with the anodic native oxide, where a fairly large hysteresis is shown which gives an effective flat-band voltage shift ΔV_{FB} of about 15V for the applied field of 1.1 x 10^6 V/cm. This hysteresis has an opposite direction from that of the positive-ion instability in Si-SiO_2, and can be explained by a trap filling mechanism where traps, distributed in the oxide, are filled and emptied by electrons tunnelling from and to the semiconductor.

The large frequency dependence of the capacitance, even in the accumulation region seems to indicate that an incompletely

oxidized and therefore fairly highly conducting layer is present near the interface which effectively reduces the oxide thickness at low frequencies (the classical Maxwell-Wagner effect (20)). The presence of such a layer has been actually confirmed by Itoh et al (18) in the case of Al_2O_3 - GaAs and SiO_2 - Al_2O_3 - GaAs interfaces using ellipsometric means and has been termed a "meta morphic layer". Sugano et al (1) have also shown by plasma oxidation of GaAs (a gaseous analogy of anodization) that a native oxide with a fairly low resistivity (10^8-10^{10} Ωcm) is formed under a very rapid growth condition. A simple analysis of the experimental data suggests that the "meta morphic" layer should have a thickness of 150-200Å with a resistivity of around 10^8 Ωcm in the present case.

The positive voltage branch of the C-V curve in Figure 4.4 shows an effect typical of deep depletion for a sweep speed of the field plate voltage of 2.6 V/s, indicating a slow generation rate of minority carriers in GaAs. A similar effect has been reported in the case of GaAsP (21). This dynamic behaviour disappears, of course, as the sweep speed is reduced. Also within the measured frequency range down to 100Hz, only a so-called "high frequency" characteristic has been observed which is again consistent with the slow generation rate of minority carriers.

The effect of a short-time, relatively low-temperature annealing of such an oxide is shown in Figure 4.5. Hydrogen gas was used because low temperature annealing (~500°C) in H_2 is known to be very effective in Si MOS technology to reduce fast interface states owing to a certain complexing mechanism of structural defects which are the origin of such states (22). Remarkable improvements are clearly seen by comparing Figure 4.4 with 4.5. The hysteresis has been reduced by a factor of 15 in terms of V_{FB} for the same field strength, which means roughly a reduction of the slow trap density by the same factor. The frequency dispersion of the capacitance is also almost reduced to zero, which indicates an extinction of the "meta morphic layer". Estimates of fast interface-state densities N_{ss} have been conveniently made from the difference between the high-frequency capacitance C_{HF} and low-frequency capacitance C_{LF} through the following equation (23).

$$N_{ss} = \frac{C_i}{q} \left| \frac{C_{LF}/C_i}{1 - C_{LF}/C_i} - \frac{C_{HF}/C_i}{1 - C_{HF}/C_i} \right| \quad (1)$$

where C_i is the insulator capacitance. The result for the annealed oxide shown in Fig. 4(b) is that N_{ss} is about $6 \times 10^{11} cm^{-2} eV^{-1}$ near mid-gap.

The improvement which has been achieved by annealing is in sharp contrast to previous reports on deposited oxides where annealing has been found ineffective, and seems to suggest the importance of having a "native" oxide in order to obtain a natural and less defective interface structure.

Extensive annealing experiments, using various annealing temperatures and times, have shown that the optimum annealing temperature for such a native oxide is around 300°C. Annealing at 400°C for 1.5 hr. in H_2, reduces the oxide thickness by about 30% and completely changes the oxide color, possibly by the sublimation of As oxide (24). Although the oxide still seems very uniform the breakdown voltage is reduced to 1.5×10^5 V/cm and the direction of the C-V hysteresis is reversed.

On the other hand, no appreciable change in oxide thickness color or dielectric properties has been observed after times as long as 6 hours of annealing at 300°C in H_2 gas. The effect of annealing has been found to be very reproducible. The best result so far obtained by a longer annealing time is summarized in Table 4.2.

The result in Table 4.2 certainly indicates the large potentiality of the anodic oxide towards various MOS applications on GaAs. Therefore, further systematic study is urgently needed in the future to establish the most suitable processing of such a native oxide, optimizing the growth conditions and post growth annealing conditions (gas species and temperature). Another important feature is the stability study of the oxide where electrical, chemical and thermal stability should be established and optimized, including the bias-temperature treatments which have not been done so far. On the basis of

the results reported in Chapter 2 and also of work by Cooper et al (16), both of which indicate that the widely accepted model of a MOS capacitor (25) becomes inadequate in the case of GaAs, a more appropriate model of GaAs MOS capacitors should also be developed, using the results of more detailed C-V and conductance measurements.

A certain work on the actual MOS device fabrication using the present oxide has already been started and will be briefly reported in Chapter 7.

4.4. A New Double-Oxide Structure using Anodization Technique

As compared with SiO_2 obtained by the thermal oxidation, the present anodic native oxide of GaAs has a poorer chemical and thermal stability. It dissolves into most of the acid and base solutions. The as-grown oxide is etched even by pure water although it occurs extremely slowly (below 10^{-2} Å/sec). Such a property could be useful in certain applications such as the controlled etching of GaAs (4) but, in general, it imposes a certain limitation on the processing application. Fortunately, it does not dissolve into usual organic solvents and halogen-alcohol etchants of GaAs both of which are very useful properties for such applications. It has been also shown that the heat treatment of the present oxide above 350°C results in a change in the oxide itself, leading to deterioration in the dielectric and interface properties. Although 350°C is much higher than the usual device operation temperatures, such a property again imposes a severe limitation on device processing such as diffusion and ohmic-contact alloying, and could also have an effect on the long-term stability of devices.

The present native oxide is thought to be a glassy mixture of gallium oxide and arsenic oxide as has been demonstrated by Feldman et al for a similar oxide (24). The chemical and thermal instability of the oxide is most probably coming from the arsenic oxide part which is apparently the glassy network former of the present oxide, judging from the known properties of gallium oxides and arsenic oxides.

The essential question would be now how one can possibly enhance the chemical and thermal stability of such an oxide

without losing its favourable dielectric and interface properties.

One thing which has been tried towards such a purpose is to form a double-oxide structure by depositing an Al film on GaAs and subsequently anodizing both of Al and GaAs by a suitable choice of the anodization voltage. It has been found that such a double-oxide structure can be easily fabricated using the new electrolyte for GaAs. The point when the anodization proceeds into GaAs after finishing the anodization of Al is clearly distinguishable on the anodization current-voltage characteristics. The growth rate of Al_2O_3 film has been found to be about 10Å/V. The dielectric properties of such a double-oxide structure have been found even better than those of the native oxide, and the C-V measurement on the as-grown oxide showed curves similar to those shown in Figure 4.4. It has been also confirmed that such a structure actually improves the etch-resistance of the oxide in a remarkable way. A systematic study on the thermal stability is now going to be undertaken.

Another interesting and promising way of producing a double-oxide structure will be, for instance, to grow a iso-type GaAlAs layer epitaxially on the GaAs, in a way similar to that described in the previous chapter, and subsequently to anodize both of the GaAlAs and GaAs layers. As has been already mentioned, the native oxide of GaAlAs is more stable than that of GaAs. Thus, such an approach will provide, to a certain extent, a useful means to incorporate other elements into a glassy system to improve its properties.

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FIGURE CAPTIONS

4.1 Experimental set-up for anodic oxidation of GaAs.

4.2 Anodization current versus time, including the effect of HCl contamination. Electrolyte: one part of 3% tartaric acid solution (pH=6) mixed with four parts of propylene glycol.

4.3 Thickness versus applied voltage. Electrolyte: one part of 3% tartaric acid solution (pH=6) mixed with two parts of propylene glycol.

4.4 C-V curves of a MOS capacitor for the as-grown oxide.

4.5 C-V curves for a MOS capacitor after annealing at 300°C.

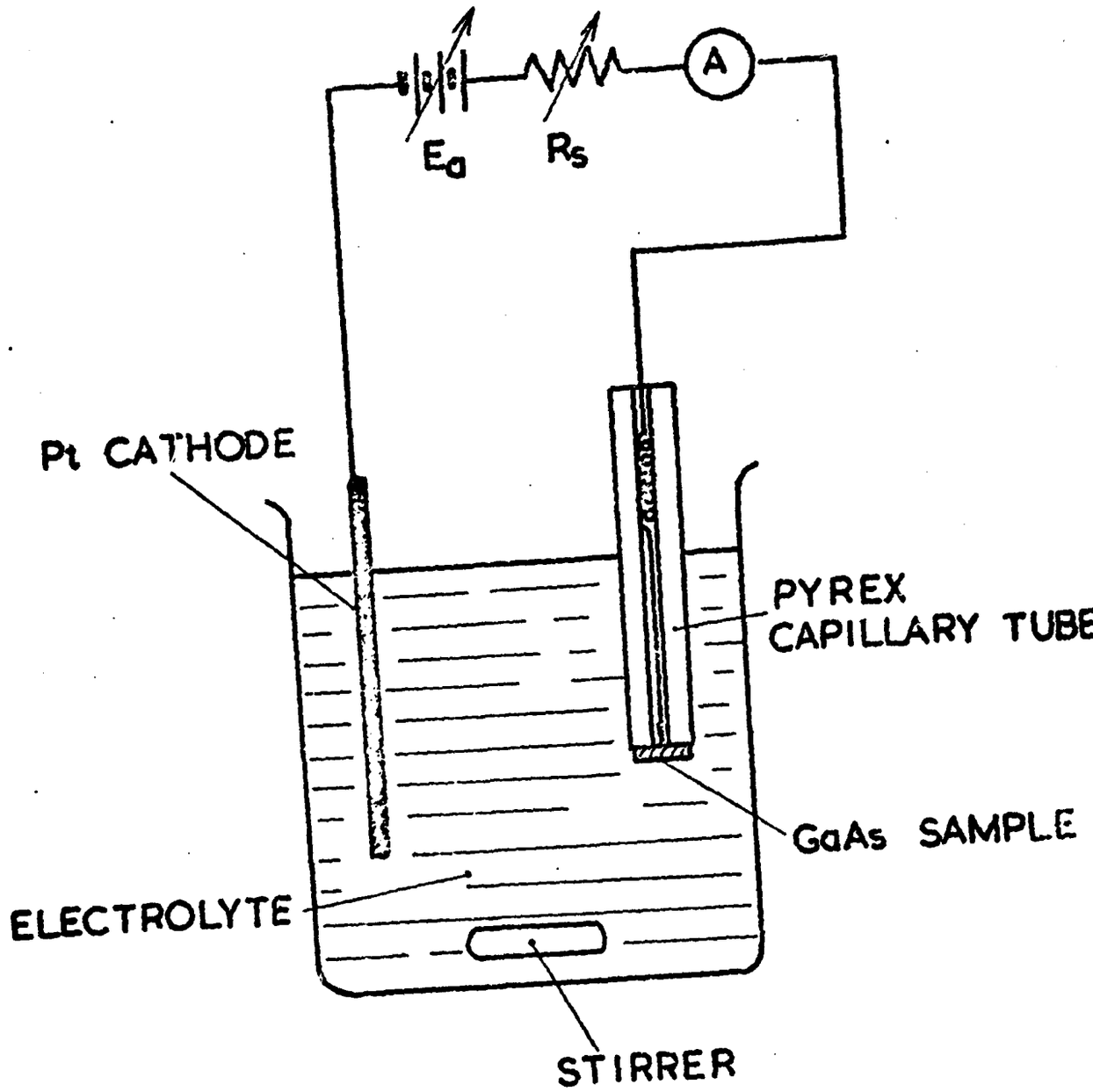


Fig. 4.1

Experimental set-up for anodic oxidation of GaAs

Fig. 4.2

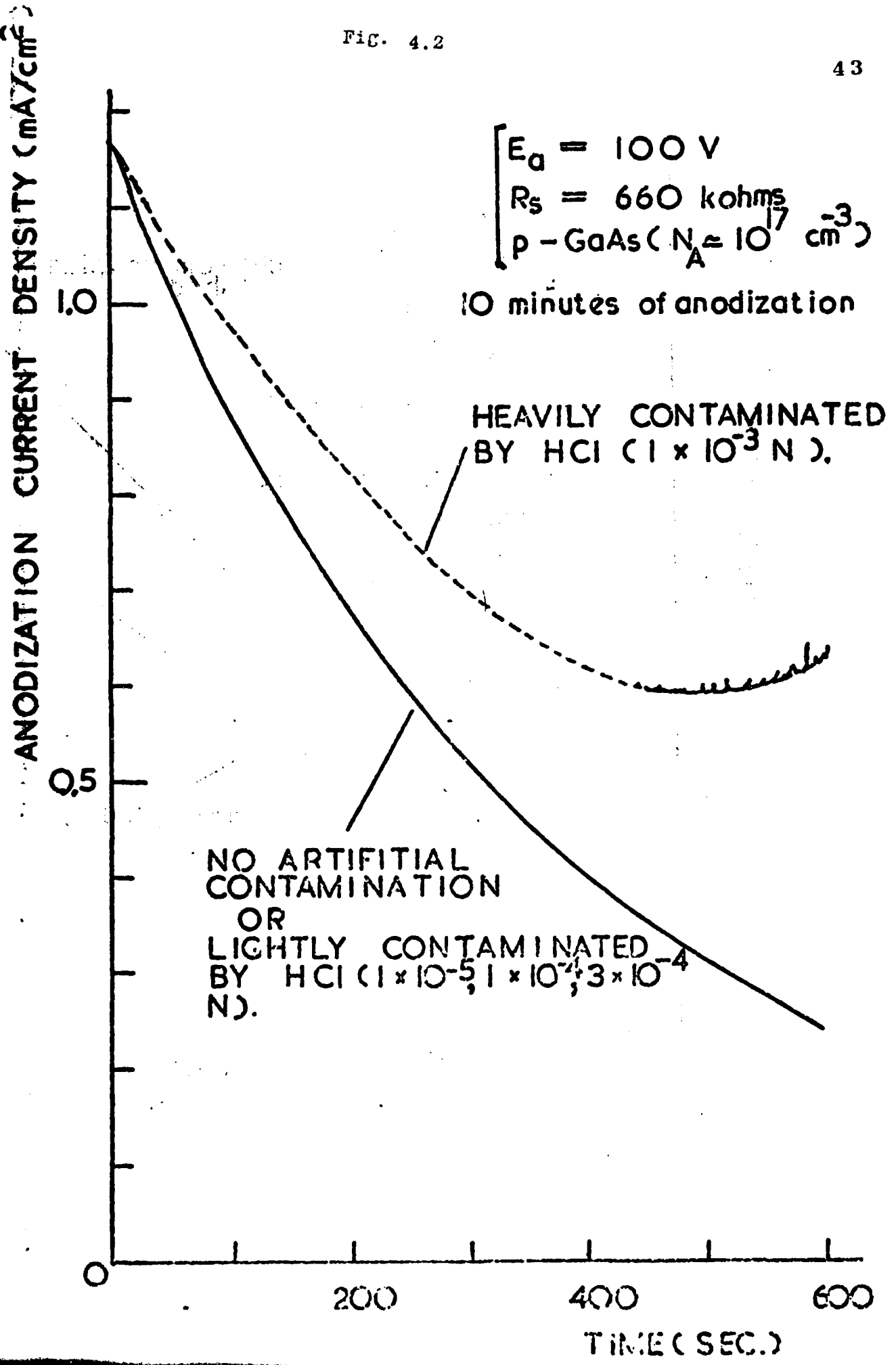
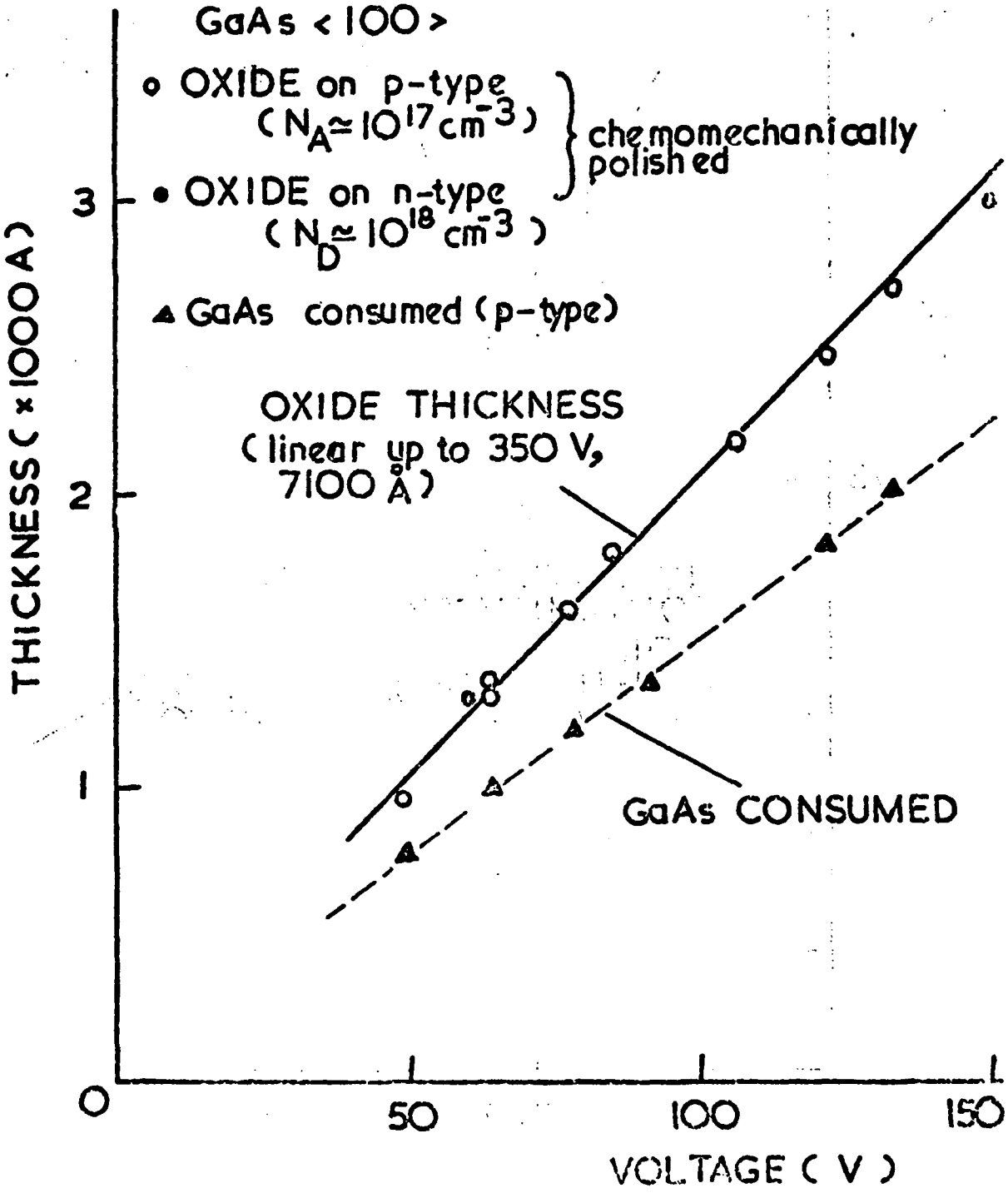

ANODIZATION CURRENT DENSITY (mA/cm²)
1.0
0.5
0
200
400
600
TIME (SEC.)
E_a = 100 V
R_s = 660 kohms
p - GaAs ($N_A \simeq 10^{17}$ cm^{-3})
10 minutes of anodization
HEAVILY CONTAMINATED BY HCl (1×10^{-3} N).
NO ARTIFITIAL CONTAMINATION OR LIGHTLY CONTAMINATED BY HCl (1×10^{-5}, 1×10^{-4}, 3×10^{-4} N).

Fig. 4.3

Thickness versus applied voltage. Electrolyte: one part of 3% tartaric acid solution (pH=6) mixed with two parts of propylene glycol



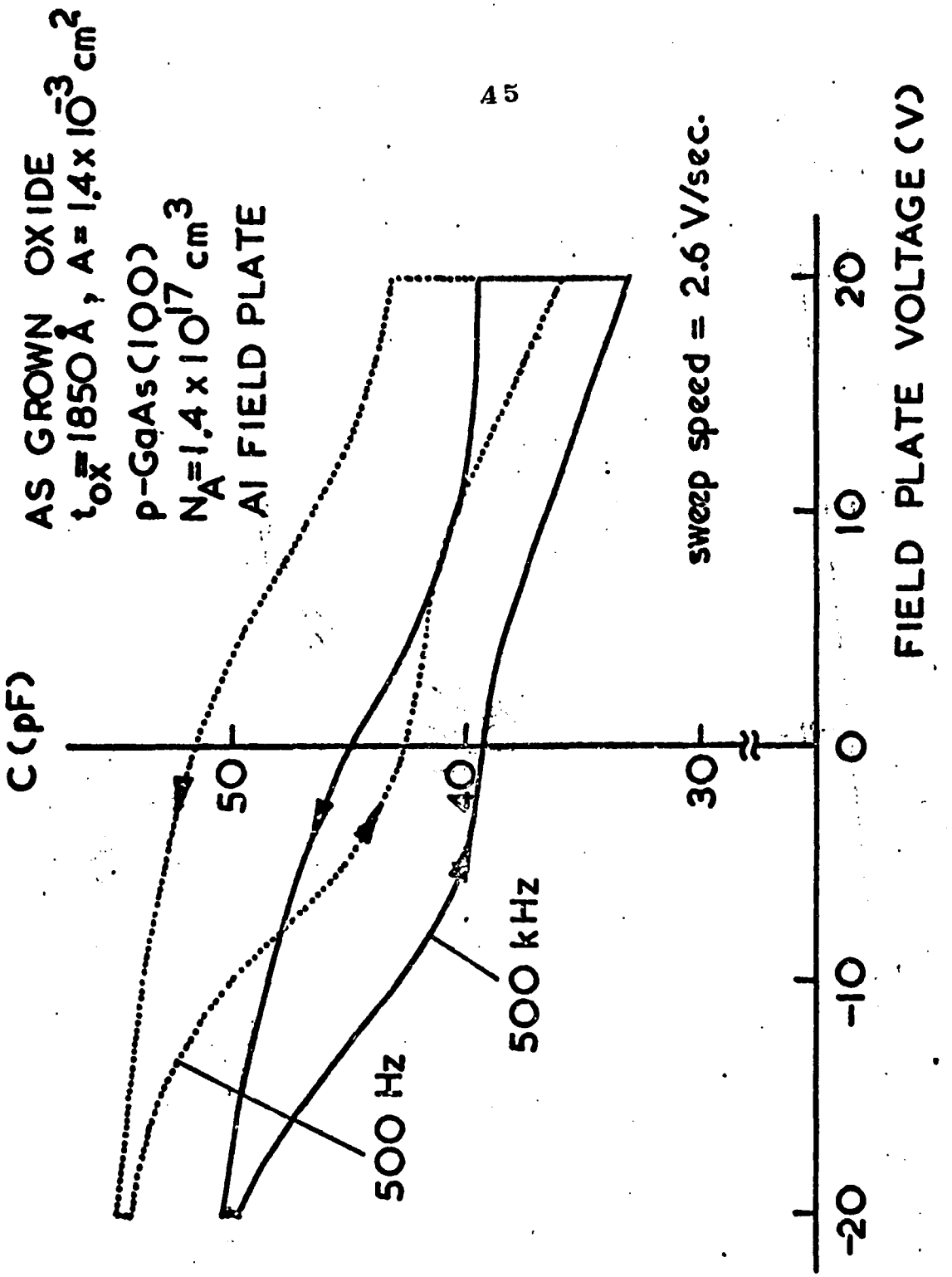


Fig. 4.4

C-V curves of a MOS capacitor for the as-grown oxide

Fig. 4.5

C-V curves for a Mos capacitor after annealing at 300°C

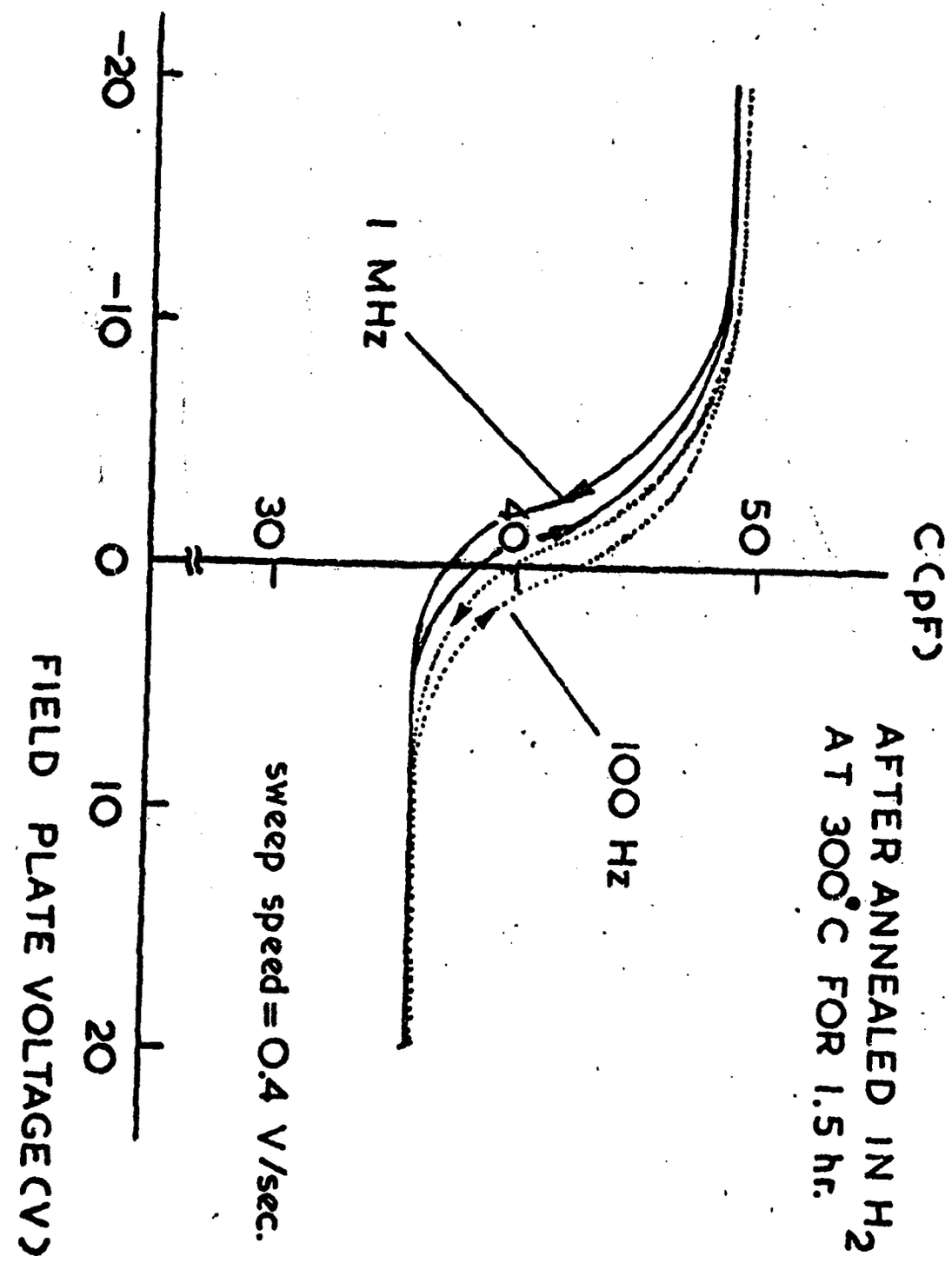


TABLE 4.1

INTERFERENCE COLOURS OF ANODIC NATIVE OXIDE OF GaAs

condition : observed perpendicularly
under fluorescent light

thickness Å	colour
500	brown
800	dark violet
1000	royal blue
1300	light blue
1600	light green
1700	yellow
1800	gold
2200	red purple
2400	dark blue
2700	green

TABLE 4.2

INTERFACE PROPERTIES IMPROVED BY ANNEALING IN H_2 GaS

Annealing conditions	300°C for 6 hours
1. hysteresis in terms of $_{\nabla}V_{FB}$	below 400 mV for applied field of 1 x 10^6 V/cm
2. frequency dispersion of accumulation layer capacitance	change over the frequency range of 100Hz - 1MHz is below 1%
3. fast interface state density	1-2 x $10^{11}cm^{-2}eV^{-1}$ near the mid gap

CHAPTER 5

ASSESSMENT OF INTERFACE PROPERTIES

(K.E. FORWARD)

5.1 INTRODUCTION

The best method of assessing interface properties is to use C-V plots at high and low frequencies. Details of the methods of determining fast interface states N_{SS}, fixed change Q_{SS} and trap densities N_T from these curves are given in Deal (1), Grove (2), Sze (3), Castegne (4), Fahrner (5), Kern and White (6). The basic requirements are plots of $C=\frac{dq}{dv}$ against bias voltage at various small signal frequencies. The plotting of these curves point by point with the aid of a bridge has the obvious disadvantages of operator frustration and the consumption of valuable time which could be better spent on other tasks less easily automated. We therefore devoted considerable time to the development of an automatic C-V plotter.

5.2 C-V Plotting System

The details of the C-V plotting system developed is described in Appendix 1, but the specification is given again here as it is relevant to the discussion below. The system has a sensitivity of 7 mV/pF for 25 mV pp signal applied to the sample. The frequency range is from 100 Hz to 2.5 MHz and the bias voltage range is ±30 volts. The ramp can be applied at rates from 1mV/S to 5v/S, and the drift rate in the hold position is 0.01 mV/S. The instrument covers the range from 0 to 100 pF but could be modified to extend this range to higher values if necessary.

5.3 Application

The instrument is usually used to plot small signal capacitance against bias voltage but it can also be used for the slow ramp technique of Castegne (4) to obtain low frequency C-V curves. By applying a step instead of a ramp and then observing C as a function of time, the retention time of MOS capacitors can be measured, Sah and Fu (7), (8). This is a useful technique for assessing the usefulness of MIS systems

for CCD applications.

5.4 Discussion of C-V Plotter

As mentioned previously, a complete description of the C-V plotter is given in Appendix 1. It has proved a very useful tool in this work and enables extremely rapid assessment of the effects of various processes, such as annealing. Care is required in its use and in the interpretation of results as factors such as ramp speed and signal amplitude can cause spurious results. The input signal amplitude also requires careful adjustment and must not be allowed to drift as the output is proportional to the square of this voltage and is hence sensitive to very small changes. The system must also be recalibrated before each measurement as the end results such as N_{SS} and Q_{SS} are obtained from differences in two or more readings. As these might be quite small differences in the large numbers small errors due to drift in the instrument can cause quite large errors in the results. The sensitivity and zero level also change slightly with frequency so it is essential to recalibrate before each reading and especially if the frequency has been changed. Due to the very small signals used and the high gain of the signal amplifier shielding from mains hum and stray electromagnetic signals is essential if errors from this source are to be avoided.

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CHAPTER 6

ADDITIONAL PASSIVATION SCHEMES INVESTIGATED

6.1 INTRODUCTION

The four main techniques available for the deposition of insulators are:-

(i) Vacuum deposition (sputtering or evaporation)
(ii) Liquid coating followed by solvent evaporation or chemical reaction which converts the liquid to a solid
(iii) pyrolitic decomposition of suitable gases
(iv) Deposition of an element followed by anodic oxidation.

It would also be possible to carry out the oxidation in (iv) pyrolitically but the sublimation of As from GaAs at relatively low temperatures precludes this method. Method (iii) has also been excluded by us on the same grounds but has been attempted by others(1) with limited success.

In this chapter, additional passivation schemes investigated are briefly described. They include four different ways of insulator deposition, i.e. use of spin-on SiO_2, Al_2O_3 deposition by anodization, electron-gun evaporation of Al_2O_3 and a precipitation of As_2O_3 layer from a liquid solution. They also include a different way of native oxidation using a NaOCl solution and also a somewhat different approach of using proton bombardment. Some of them have turned out less promising and some seem still worthwhile pursuing further.

6.2 Spin-on SiO_2 films (K.E. Forward)

An attempt was made to use Silicafilm, a product of the Emulsitone Company, which employs method (ii) above to coat GaAs with SiO_2 using the following procedure. The GaAs in wafer form was polished to a mirror finish using a chemomechanical polishing technique. Then the surface of the GaAs was etched in a polishing etch of either Br-methanol or $NH_4OH : H_2O_2 : H_2O$

to remove the possibility of Na ion contamination. The surface of the GaAs was then oxidized by exposing it to O_2 for one hour at 500°C. This latter step was necessary to ensure the adherence of the SiO_2 film. The silicafilm suspension was then applied to the GaAs and reduced to a 2000Å thick film by spinning at 6000rpm. The resulting SiO_2 film was then baked at 90°C for one hour and finally sintered at 250°C for two hours. Al field plates, about 400μm diameter were then evaporated through a metal mask to form field plates. Capacitance and conductance were then determined with bias voltage as a parameter, using a Boonton Bridge. Then using the method of the conductance technique by Nicollian and Goetzberger (3) the density of fast interface states Nss was determined. The results were not encouraging for many reasons.

The disadvantages of spin on oxide were that it did not coat evenly, due to edge build up which is not very serious and to channeling of the solution from the centre during spinning which is much more serious as it resulted in radial ridges in the final film. The film of SiO_2 did not adhere to the etched GaAs without pre-oxidation as described above and this means that the undesirable double layer hysteresis effects reported by various workers (4) (5) are unavoidable. The SiO_2 films also craze if heated to temperatures above 500°C, due to differential expansion at the GaAs and SiO_2 interface, unless the SiO_2 films are less than 2000Å thick. The density of interfaces states, N_{ss}, was also rather high at $2 - 4 \times 10^{12}$ cm^{-2} eV^{-1}. In some cases spin on SiO_2 films may be of some use and N_{ss} may be reduced by annealing but due to the fact that we have developed more successful techniques the method was abandoned after these initial experiments.

6.3 Anodization of Al (K.E. Forward)

The vacuum deposition of Al is extremely simple and can be carried out using either an electron beam gun or a resistive heater such as a 3 or 5 core tungsten wire hairpin coil or basket. This is in strong contrast to Al_2O_3 which is a refractory material which can only be successfully evapoured in an e-gun. The ease of Al deposition therefore makes the

technique of depositing Al and subsequently anodizing it to produce an Al_2O_3 film most attractive. There are many reports in the literature on the anodization of Al and provided a suitable electrolyte is used extremely dense film with excellent electrical properties can be grown (6) (7) (8), as also described in Chapter 4.

Before we succeeded with our new anodization of Chapter 4, there were several negative results. Using the electrolyte specified by Francis (6) or that of Davies (7) we were able to anodize Al on glass. However, when Al on GaAs was used as the anode, the only result achieved was the etching of the GaAs and this removed the Al_2O_3 film. H_2O_2 30% aqueous solution as reported by Logan et al (9) was then tried but due to the effect of impurities this also failed to produce the desired results. The failure of H_2O_2 as an electrolyte for this purpose is not surprising as Logan et al reports that as little as 2 p.p.m. of strong acid is sufficient impurity to convert the anodization into etching . We could not even obtain H_2O_2 of that purity.

From the experiments it was concluded that in order to be able to anodize Al on GaAs an electrolyte would have to be found which could be suitable for GaAs as well as Al. H_2O_2, which was then the only known electrolyte in which GaAs could be anodized, requires such high purities that it is not a very practical solution. Only the anodization of GaAs in a glycol electrolyte, as described in Chapter 4, produced positive results, producing a highly corrosion-resistant double-oxide structure.

6.4 e-gun evaporation of Al_2O_3 (K.E. Forward)

Although Dr. Hill at the Newcastle Polytechnic gave us much of his valuable time we were not able to obtain useful results with his equipment. Firstly alumina proved to be an unsatisfactory source due to outgassing. It was therefore decided to use single crystal Al_2O_3 in the form of artificial ruby. The problem was attempted with the help of another local laboratory and Al_2O_3 was successfully deposited. However, the electrical assessment has not yet been completed and the results are going to be reported at a later date.

6.5 Passivation with As_2O_3 (B. Weiss)

It has been shown by Kyser and Millea (10) that the chemical etching of GaAs in concentrated nitric acid solutions produces a layer of arsenic oxide on the surface of the sample.

Several samples of (-111) orientated GaAs were etched at room temperature in a nitric acid solution, containing one part conc. HNO_3 with one part distilled H_2O by volume, for five minutes. The resulting oxide layer was examined in the S.E.M. Due to the insulating nature of the sample surface it was coated with a 300Å thick layer of gold to prevent it charging up. S.E.M. micrographs of the surface of the sample are shown in Figure 6.1 and they show that these layers are quite flat although considerable work is required to produce more uniform layers suitable for MOS devices and surface passivation.

6.6 Native Oxidation of GaAs using an aqueous solution of NaOCl. (H. Hasegawa)

During some studies done in this laboratory by Hartnagel and Weiss (2) of etch polising methods, it was discovered that sodium hypochlorite is a dislocation-revealing etch for (111) GaAs and that it produces after some initial etching a stable and reasonably etch resistant thin native oxide layer. It certainly means that this etchant removes only GaAs during the initial period. Sodium hypochlorite is therefore primarily employed for etch polishing when the oxide formed is continuously removed by mechanical action. It was obvious that this solution should be further explored in connection with its oxidizing property.

As a result of further study, it has been confirmed that a stable and highly etch-resistant thin native oxide layer can be formed by placing polished GaAs chips into a dilute aqueous solution of NaOCl with a volume mixing ratio of typically from 20:1 to 50:1. The resulting layer is opaque with a whitish colour. It shows, under a microscope, a crystallite structure rather than a vitreous state. The film thickness obtainable by this method is restricted to several hundred angstroms, possibly because the oxidizing agent cannot diffuse through the grown native oxide layer. More concentrated solutions have been

tried to increase thickness, but it resulted in very dull surfaces.

The highly etch-resistant nature of such a film is certainly interesting as compared with the chemical properties of the anodic native oxide described in Chapter 4 where the oxide is readily soluble to most of acid and base solutions. It seems to suggest that during the oxidation by NaOCl As atoms of GaAs dissolve into the solution in a certain form of oxide, whereas Ga atoms remain on the surface, being oxidized and form a very stable crystal structure such as β-Ga_2O_3 or similar structure including Na or Cl. A glassy structure cannot be formed because basically the Ga atom is not a glass network former while the existence of glassy As_2O_3 is well known. As_2O_3 is also known to dissolve into water depending strongly on pH (11). However the above explanation is only a speculation and needs, of course, a detailed chemical analysis.

In conclusion, this approach of native oxidation has now turned out to be less attractive primarily because of the limited thickness available and the crystallite structure, where grain boundaries can have detrimental effects for the practical passivation applications, and also in view of the highly probable contamination by sodium ions which might lead to serious ionic instabilities encountered in Si MOS technology.

6.7 Passivation with semi-insulating GaAs and GaAlAs layers produced by proton bombardment (H. Hasegawa)

In connection with the epitaxial approach for the passivation described in Chapter 3, an alternative method to form a semi-insulating semiconductor material is to use proton bombardment. Use of such a technique for GaAs junction device isolation has been described by Foyt et al (12). GaAlAs can also be converted into semi-insulating shown by Pavennec et al. (13).

The actual mechanism which is responsible for such as conversion has not been established but seems to be closely related to the disorder in the crystal produced by the bombardment.

In order to see whether such a technique is useful for passivation purposes, proton bombarded n-GaAs and n-GaAlAs

samples were produced with the aid of the Physics Department at the University of Salford, U.K* The proton energy and dose used in the experiment is 40Ke V and 10^{13} 1/cm^3, respectively. According to the literatures (12) (13), the thickness of the resultant semi-insulating layer should be about 4000Å. To investigate the electrical properties, an Al field plate was provided by the standard technique. Careful electrical measurements at small bias voltages indicated the presence of a highly resistive layer. However, the breakdown voltage of such "MiS" devices have been found unfortunately very small, typically around 1V, and therefore no meaningful C-V measurements have been done so far. Within the measured range, no appreciable change in the capacitance was observed.

The present results seem to indicate that the technique of proton bombardment is not suitable to "MiS" applications, or insulation of metalization patterns as is employed in Si planar technology. However, for the purpose of producing an "electronically" passivated surface with reduced interface states and traps, the question must be more carefully investigated because such a technique could still provide a better interface as compared with the exposed air-GaAs interface which would have an interface state density larger than 10^{13} 1/cm^3. If the usual dose of 10^{12}-10^{13} 1/cm^2 has actually a one-to-one correspondence to the electronically active disorders in the semiconductor and the carriers in the active semiconductor can make frequent charge transfers across all these defects, there is no hope, but; these assumptions seem unlikely to hold. In fact, there is a certain experimental evidence that the performance of GaAs devices, in particular, Impatt devices, can actually be improved by proton bombardment along the device periphery. Further study is therefore required to clarify the interface properties of proton bombarded GaAs layers.

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*We should like to express our gratitude to Professor G. Carter and Dr. W. Grant of the University of Salford where our slides were proton bombarded.

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FIGURE CAPTIONS

6.1 SEM micrograph of arsenic oxide layer.

Fig. 6.1
S.E.M. micrograph of arsenic oxide layer

CHAPTER 7

FABRICATION OF DEVICES

(K.E. FORWARD)

The fabrication of two devices is currently in hand, an MOS transistor and CCD. Both of these will be made in GaAs using the GaAs/(GaAs) Oxide described in Chapter 4 to obtain planar structures. The work so far carried out on the FET is described first as this is more advanced than the CCD.

7.1 GaAs-MOSFET

A GaAs-MOSFET has been fabricated on an epitaxial layer 9μ thick on an n-substrate, using native oxide insulation. The fabrication details are given here to provide a convenient reference for workers at these laboratories who will continue this work.

7.1.1. Fabrication

The mask set is shown in Figure 7.1. The process steps are given in Figure 7.2 but a few extra notes are needed to avoid repeating mistakes of the past. In steps 3 and 4, the anodization rate of 21Å/Volt is used to determine oxide thickness where the voltage is that measured between the sample and the cathode at a current of 20μA. The films have in some cases been grown at constant current density of about 50 mA cm^{-2} but the current has always been reduced to 20μA to determine the formation voltage. When photo-lithography is used in any photolithographic step it must be remembered that the Shipley developer is a strong base which rapidly dissolves the (GaAs) oxide. This is useful as the photo-resist can be developed and the windows opened simultaneously.

Another point that must be made is that when using the Shipley 1350 the developer needs to be mixed 1 : 4, resist : water, in order to be strong enough to develop the very narrow gaps used in these masks. The standard 1 : 10 mixture is too slow to ensure complete development. For

both Shipley and Kodak resists 20 sec. exposure times have been used. An unfortunate feature of the native oxide is that it reacts with Sn above 232°C to produce an almost insoluble powder which is extremely difficult to remove from the GaAs. Alloying of the Sn:Ag junctions must not be carried out using GaAs (Oxide) as a mask for this reason. Before any further progress can be made on this project both negative and positive mask sets are required to ensure complete freedom of choice of resists, because in some cases Kodak Micro-neg-resist must be used as it has the advantage of developing in an organic liquid which does not attack GaAs (Oxide). Yet in other cases Shipley resist must be used as it is readily soluble in acetone while Kodak resist is softened by boiling trichloro-ethylene and removed with a cotton bud. In step 1 the drain and source metalizations are delineated using the Shipley resist float-off technique. The native oxides have been successfully grown using 50 mA/cm^2 anodization current and measuring the formation voltage at a current of 0.5mA/cm^2. The oxide will then be 21Å thick per volt.

7.1.2 Discussion of MOS fabrication

The main problems encountered are concerned with the photolithography. The most obvious problem from the above is the harsh caustic developer used with Shipley resist. It would be much better to work with Kodak Micro-Neg. or Emulsitone resist. The Kodak resist uses organic solvents for its developer and for its rinse, while the Emulsitone resist develops in water. These resists are both negative and so our mask set is unsuitable. It would be well worthwhile making a new set suitable for negative resists, as both Kodak Micro-Neg. and Emulsitone are stocked by this laboratory. The 10μ line width for the diode windows is too narrow and needs to be opened up to at least 20μ and probably to 30μ. Masks which have 10μ lines only on them also require aligning marks at least 30μ wide, as it is impossible to observe the surface of the chip through a 10μ wide slot. These problems of line widths and alignment marks could be overcome at the time the negative masks are produced. This is not to say that the present set of masks is impossible to use but they are more difficult to use than they need to be. Fabrication of this MOSFET has taught us a lot about device processing using native oxide as an

insulator and mask and this experience will be invaluable when the CCD's are fabricated.

7.2 Charge Coupled Device (CCD)

The CCD is essentially an interdigitaled electrode structure with a very fine inter-electrode spacing. (An excellent review of CCD technology and application is contained in the International Conference Proceeding, Technology and Applications of CCD's, Edinburgh 1974). In order to achieve this very fine spacing we intend to deposit one set of electrodes using Au which will then be covered by several hundred Å of Al, which will then be anodized. The second set of electrodes will then be deposited overlapping the first. The spacing of the electrodes at the surface of the insulator will be determined by the thickness of the oxide layer which will be 500 to 1000Å thick, giving a very fine spacing indeed. In addition to the narrow spacing a stepped gate structure as required for 2-phase operation is also obtained. The set of processing steps is similar to that shown in Figure 7.2 and an explanation of each step is already given. The mask set for an 8 cell CCD and a set for a 64 cell CCD have been cut and are shown in Figure 7.3 and Figure 7.4. This work will be continued by Mr. Bayraktaroglu.

FIGURE CAPTIONS

7.1 Mask set for A GaAs MOSFET.

7.2 Process Steps of MOSFET fabrication.

7.3 Mask set for a 8 cell GaAs CCD.

7.4 Mask set for a 64 cell GaAs CCD.

Fig. 7.1

MASK SET FOR A GaAs MOSFET

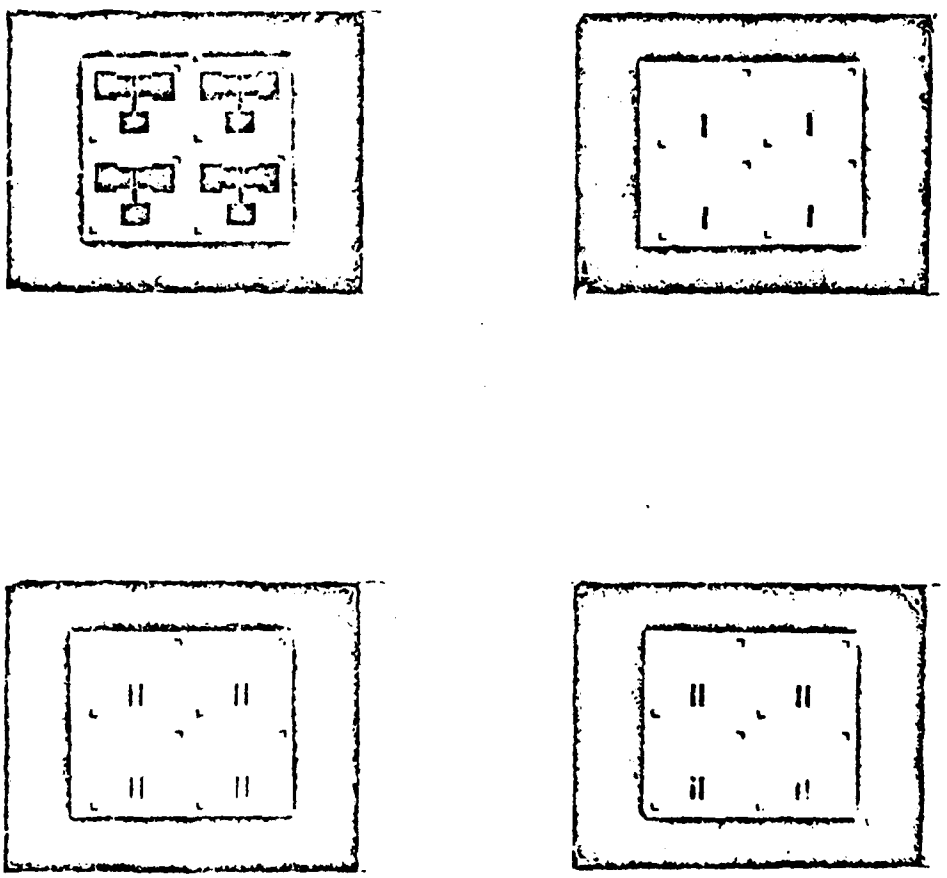


FIGURE 7.2.

PROCESS STEPS FOR MOSFET

Step 1. Alloy drain and source junction using mask 1 to obtain 30μ wide Sn:Ag drain and source stripes.

Step 2. Cover with 1000Å of Al.

Step 3. Anodize GaAs except gate area to depth of 4-5000Å native oxide.

Step 4. Anodize gate area with 500Å native oxide.

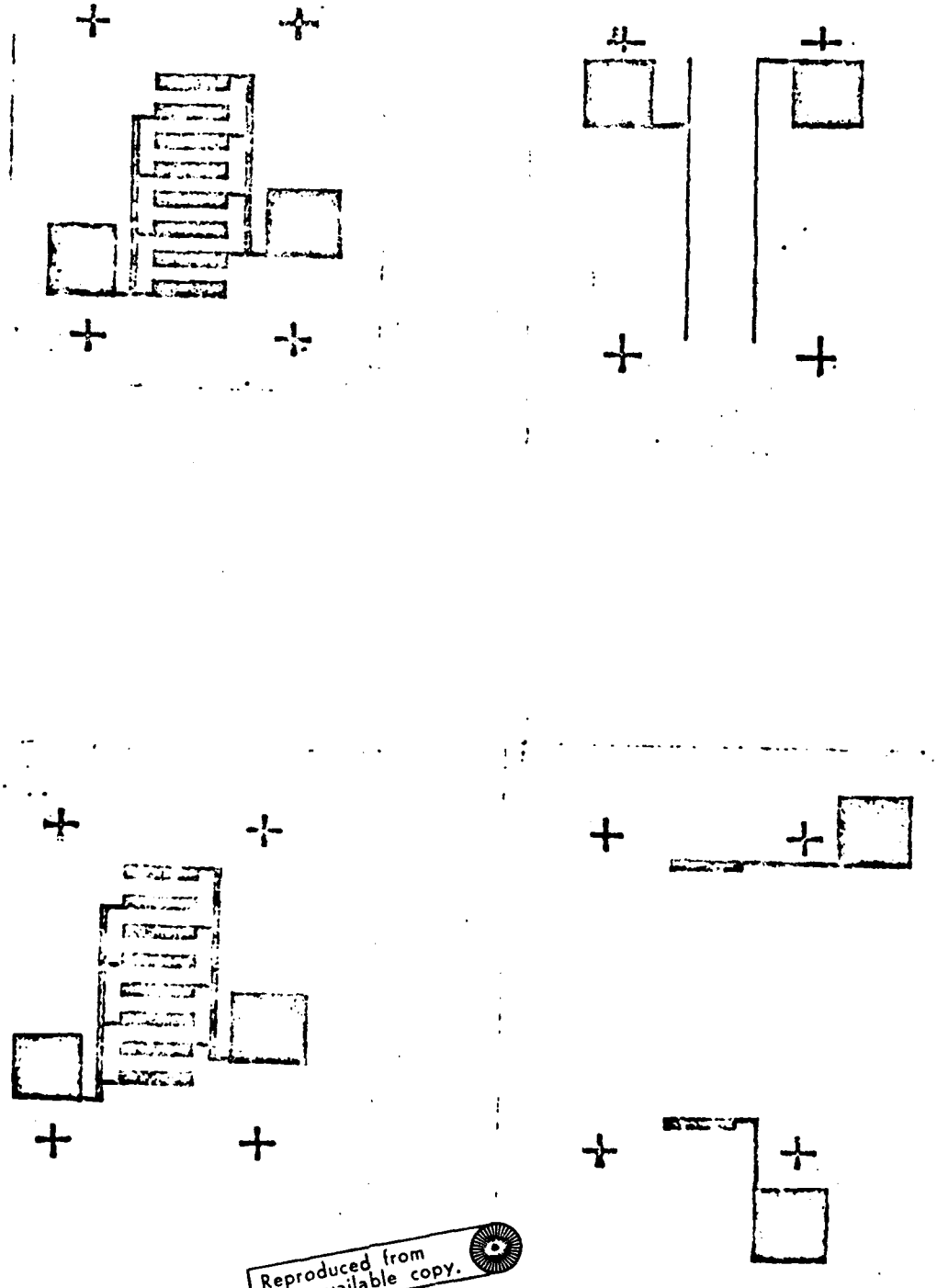
Step 5. Deposit 1000Å of Al and anodize.

Step 6. Delineate drain and source contacts using mask 2 and expose GaAs under gate.

Step 7. Deposit drain source and gate contacts using mask 4.

Fig. 7.3

MASK SET FOR A 8 CELL GaAs CCD



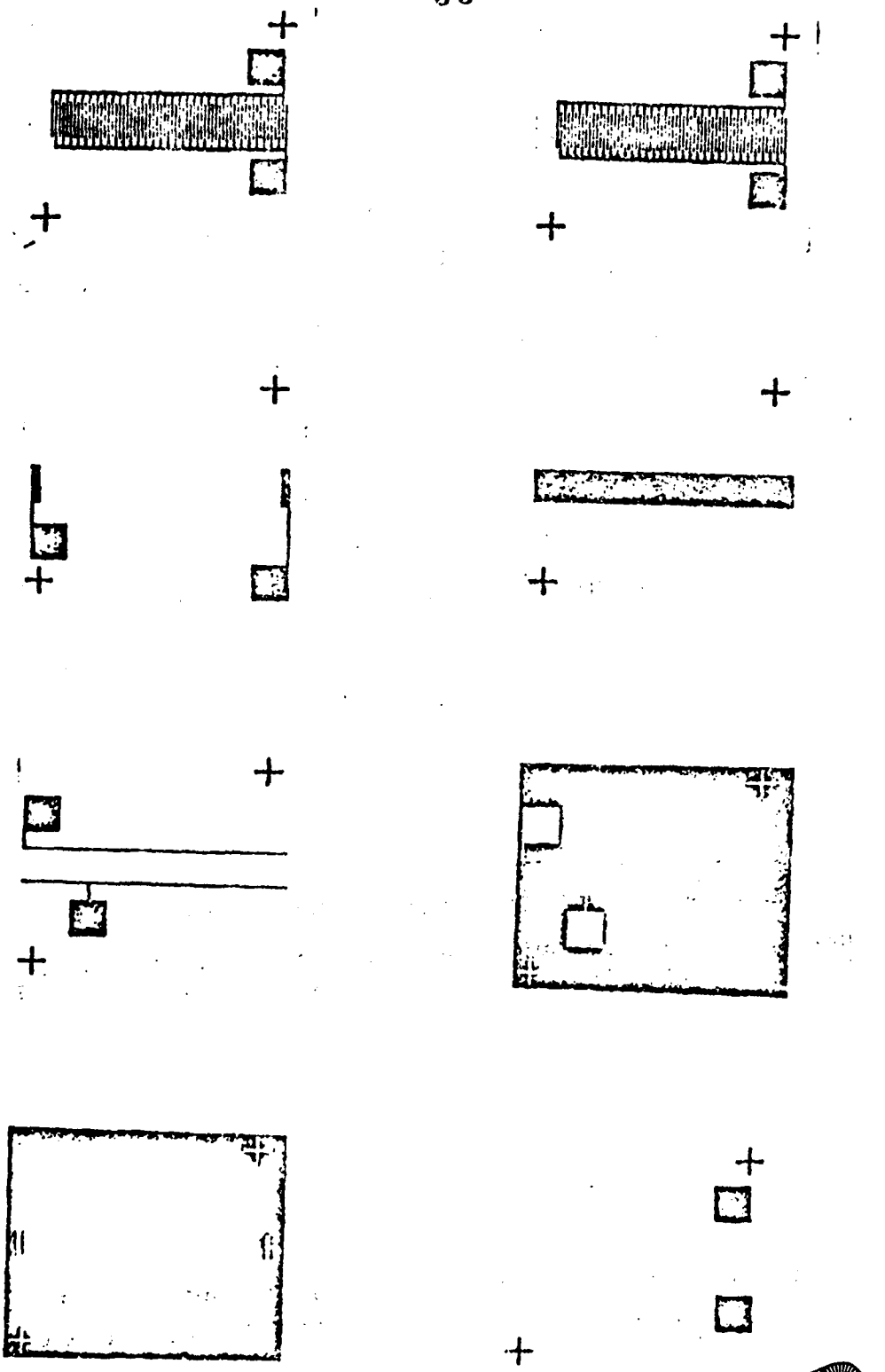


Fig. 7.4

MASK SET FOR A 64 CELL GaAs CCD

APPENDIX I

AN AUTOMATIC C-V PLOTTER

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ABSTRACT

A C-V plotter is described which employs a novel current sensing circuit to enable the plotting of incremental capacitance, $\frac{dQ}{dV}$, as a function of bias voltage. The main advantages of this current sensing circuit are that the output voltage, which is proportional to the capacitive current through the capacitor under test, is in phase with the applied voltage and that its magnitude is independent of frequency. The product of these two terms at any signal frequency therefore contains a d.c. term which is proportional to the capacitance. Design equations are given which enable the components of this circuit to be selected. A complete measurement system based on this circuit is then described and details of particular circuits are given. Examples of plots obtained for GaAs MIS capacitors are given as examples of the application of the system.

1. Introduction

According to Deal[1] the study of insulator/semiconductor interfaces is best carried out by means of C-V plots, and there are many reports of the application of C-V plots to the determination of fast interface states, fixed charge and slow trap densities (ref. [2, 3, 4, 5, 6], for example). For the rapid assessment of device processing which involves the use of insulators on semiconductors an automatic C-V plotter is highly desirable as manual methods such as point by point plotting using a capacitance bridge tend to be tedious and time consuming. In designing such a system there are several important factors which must be considered to ensure that the instrument is versatile enough to permit those features of the C-V plots which are due to interface properties to be distinguished from effects which are introduced by the measurement technique. The nub of this problem is that the effects being observed are functions not only of bias voltage but also of time. The rate of change of the bias voltage is therefore a critical factor and consequently we have used a ramp generator, with a rate controllable over a very wide range, and have provided a hold feature which enables it to be stopped at any point for quite long periods.

The other factor which requires careful consideration is the amplitude and frequency of the small a.c. signal which is used to detect the incremental or small signal capacitance. As the study of fast interface state requires the measurement of capacitance at widely differing frequencies a novel current sensing circuit has been devised which is

independent of frequency but which still allows the test capacitor to be d.c. biased. This circuit is described in detail below and an example is also given to show the difference obtained by using various frequencies when measuring MIS capacitors.

The capacitances to be measured are usually quite small and even small changes can be quite significant so that the system is required to have a relatively high sensitivity. Some workers in this field have used the variation in detector current of a bridge circuit as an indication of the change in capacitance, but this is only linear over a limited range and is totally unreliable in MIS studies, where, as Nicollian and Goetzberger[9] point out, the conductance can vary much more rapidly than the capacitance. Another method which has been proposed by Tantraporn[7] suffers from the same disadvantage as capacitive and conductive components are not distinguished and has the added problem of having an output which is a function of frequency. We have chosen a method which enables a synchronous detector to be used, and which has an output independent of frequency. The synchronous detector ensures a high sensitivity and enables the capacitive component to be distinguished from the conductive component ensuring that the variations observed in the output can reliably be interpreted as variations in capacitance.

An added advantage of this system is that it is extremely simple, due to the fact that it can be realized using a few standard readily obtainable components.

2. Measurement System

Tantraporn[7] has described a system for measuring capacitance where a resistor is placed in series with the capacitor under test and the voltage across this resistor is taken as proportional to the capacitance. The circuit is shown in figure 1 and it can be seen by inspection that provided $R \ll 1/\omega C$ that the output voltage, v_o, will be given by

$$v_o = R \, v \, \omega \, C$$

Hence v_o is directly proportioned to C but it also varies with ω. As pointed out above this circuit also has the disadvantage of not distinguishing between the capacitance and the conductance and so is not suitable for MOS studies. The circuit in figure 2(a) shows a capacitor in place of the resistor and by inspection v_o is now given by

$$v_o = \frac{vC}{C_s}$$

provided $C_s \gg C$. This circuit has two advantages: (1) it is independent of frequency (2) v_o and v are in phase if C is a pure capacitance. When C is shunted by a conductance the component of v_o in phase with v is due to the capacitance and independent of the shunting conductance. The detection of the in phase component can be very simply achieved by detecting the d.c. component of the product of v and v_o. Although the substitution of C_s for R enables C to be easily detected, and removes the frequency dependence from the output it eliminates the d.c. path by which the bias can be applied to the test capacitor. A resistor R_s is therefore

placed in parallel with C_s and provided $R_s >> 1/\omega C_s$ it will not disturb v_o. But R_s must also not disturb the d.c. bias applied to C, so $R_s << R_{D.C.}$, where $R_{D.C.}$ is the d.c. resistance of the test capacitor, is another inequality which must also be satisfied. Figure 2(b) shows a sampling circuit which is completely satisfactory provided the following inequalities are satisfied:-

$$C_s >> C \qquad (1)$$

$$R_s >> 1/\omega C_s \qquad (2)$$

$$R_s << R_{D.C.} \qquad (3)$$

In practice these inequalities are easily satisfied for high quality insulators such as are necessary in semiconductor technologies. As an example for C ≈ 50pF and $R_{D.C.} > 10^{10}\Omega$ C_s = 10nF. and $R_s = 10^8$ ohms easily satisfy these requirements while maintaining a measurement accuracy of better than 1%, down to ω as low at 100 rad.sec^{-1}.

It has already been stated above that the most satisfactory detector for C is a multiplier with inputs v and v_o, so provided the ramp is applied through a resistor R, which does not attenuate the small signal voltage applied to the test capacitor, a complete system for C-V measurement has now been developed, and is shown in block diagram form in figure 3. The capacitor C_1 and C_2 are provided to attenuate the signal applied to the test capacitor so that the measurement is made with a suitably small voltage whilst maintaining a substantial signal at the multiplier input, and to isolate the d.c. bias from the signal generator. The output voltage from the current sampling capacitor C_s requires

considerable amplification and this can be carried out by any high gain bread bandwidth low-pass amplifier.

3. Circuit details

The circuits required to realize the system shown in figure 3 are all readily available in a variety of integrated and discrete component circuits, so the particular circuits described here constitute only one of an infinite number of possibilities. Although we were interested in small signal frequencies from 100Hz to 1MHz and hence designed our system to operate over that passage, much higher frequencies should be possible. In fact the upper limit of our system is 2 MHz.

(A) Ramp Generator

Although the waveform of the bias voltage generator is not critical in a simple C-V plotter there are many reasons which make a linear ramp generator highly desirable. The easiest way to generate a linear ramp is to apply a step input to an RC system. If the amplitude of the step is V volts and the time constant of the integrator is T then the output will be given by V/T volt sec^{-1}. Thus with a time constant of either 1 sec. or 100 sec. and an input variable from 0.1 volt to 5 volt, ramps with rates from 10 m volt sec^{-1} are possible. The circuit we have used is shown in figure 4 where a 747 amplifier with a nominal gain of 10^5 is the main source of amplification for the integrator. The single stage output amplifier using transistor T_1 is provided to enable an output swing of $\pm$ 30 volts to be obtained. The dual - F.E.T. used in the input ensures that the input offset is small and hence provides a low drift rate when the integrator is

switched to the hold position.

(B) Multiplier

An integrated Gilbert[10] multiplier which operates up to 150 MH_z has been used and is the best of the multipliers available. The potentiometers RV_1 and RV_2 are used to adjust the balance and level of the output. An operational amplifier has been added as a level shifter and low pass filter. Finally, the output is filtered using a low pass passive filter with a sharp cut-off at mains frequency to remove unwanted hum from the output. Figure 5 shows the multiplier, output amplifier and filter.

(C) Amplifier

We have used a four stage amplifier with a flat response up to 6MH_z and a nominal midband gain of 750 which is stabilized by feedback applied to each stage.

4. Application

Figure 6(a) shows some of the typical MIS curves we have obtained for GaAs/(GaAs) oxide MOS system including the effect of annealing, details of which have been reported by Hasegawa, Forward and Hartnagel[2]. These curves show the wide range of signal frequencies, bias voltages and ramp rates which are possible with this system. It is only fair to comment that the bridge measurements required several hours of a skilled operator's time while the curves plotted automatically required only a few minutes.

5. Conclusion

A novel input circuit for a capacitance vs bias voltage measurement system has been described, which enables measurements to be conveniently made over a wide frequency range. Provision has also been made for the application of d.c. bias voltage and a set of inequalities has been given to enable the sampling capacitor and shunt resistor to be chosen. Circuits by which automatic C-V plotting can be carried out using this input circuit have been given. Examples of its application to GaAs MIS capacitors are provided, which show that this system is a most useful instrument in the study of MIS structures.

6. Acknowledgement

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10. Gilbert, B., IEEE, J. Solid State Circuits SC-3, 4, p365-373 (1968).

FIGURE CAPTIONS

Figure 1. Previous input circuit[7]

Figure 2. Novel input circuit

Figure 3. Block diagram of the complete system

Figure 4. Circuit diagram of the ramp generator

Figure 5. Multiplier, output amplifier and filter

Figure 6. MOS C-V plots by the present plotter as successfully employed to study effects of annealing on anodic native oxide of GaAs.

PREVIOUS INPUT CIRCUIT[7]

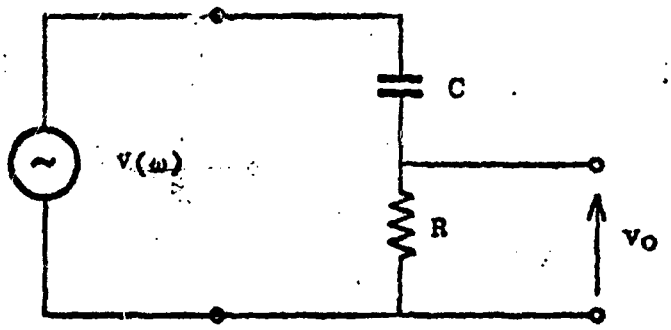

Figure 1

NOVEL INPUT CIRCUIT

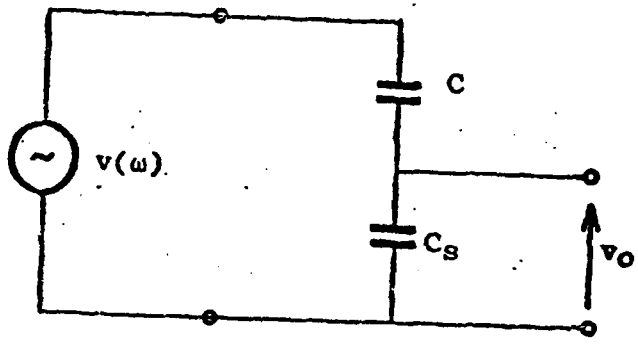

Figure 2(a)

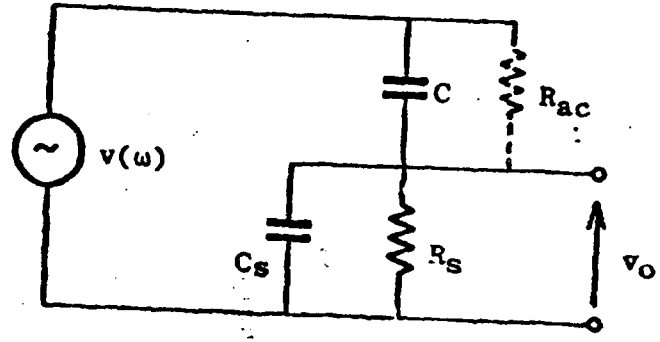

Figure 2(b)

BLOCK DIAGRAM OF THE COMPLETE SYSTEM

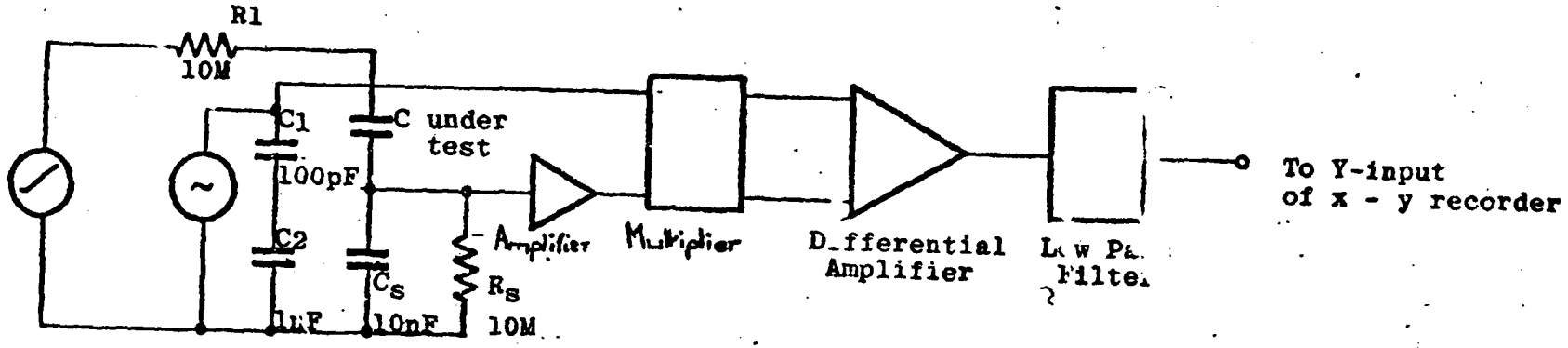

Figure 3

CIRCUIT DIAGRAM OF THE RAMP GENERATO

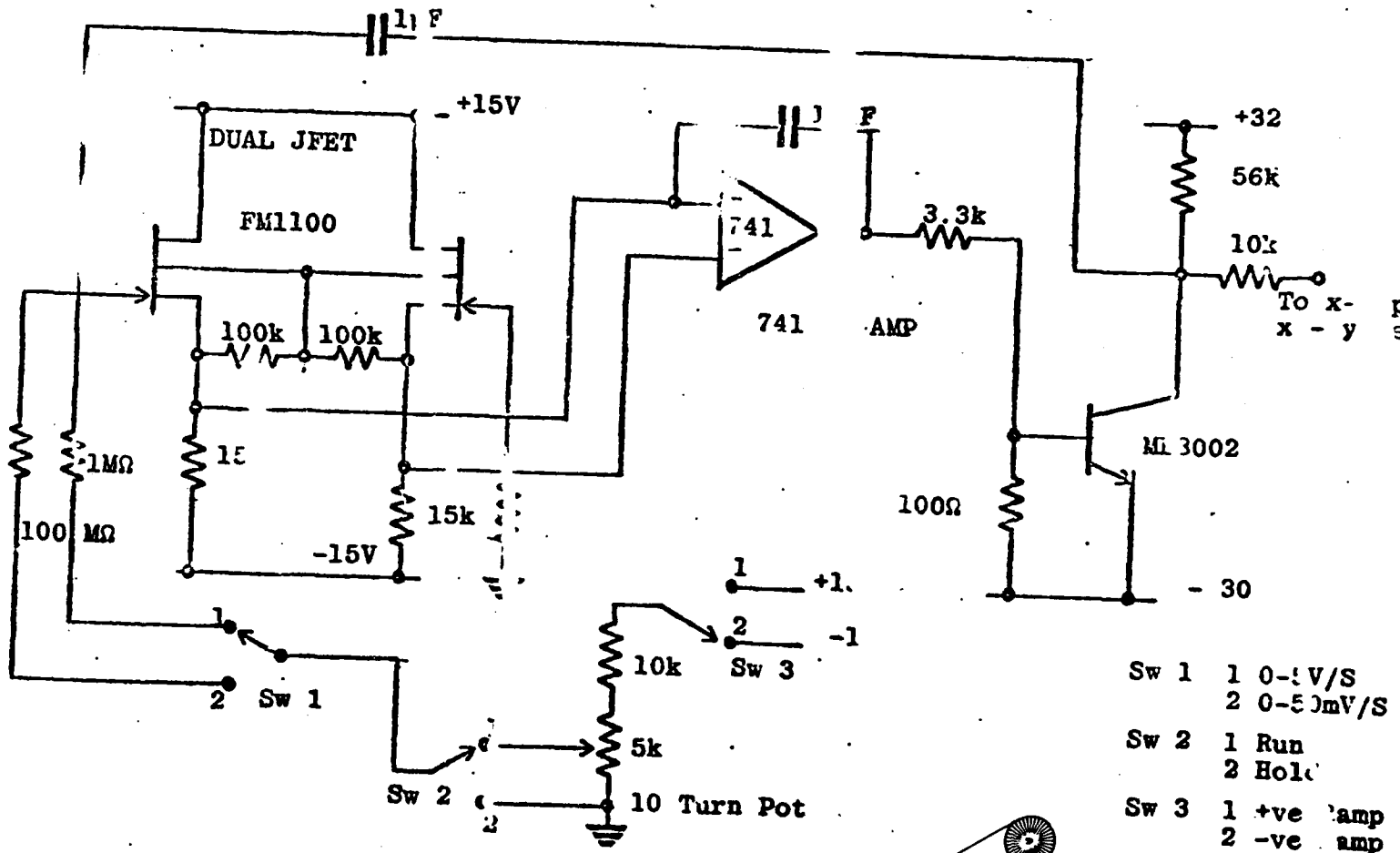

Figure 4

MULTIPLIER, OUTPUT AMPLIFIER AND FILTER

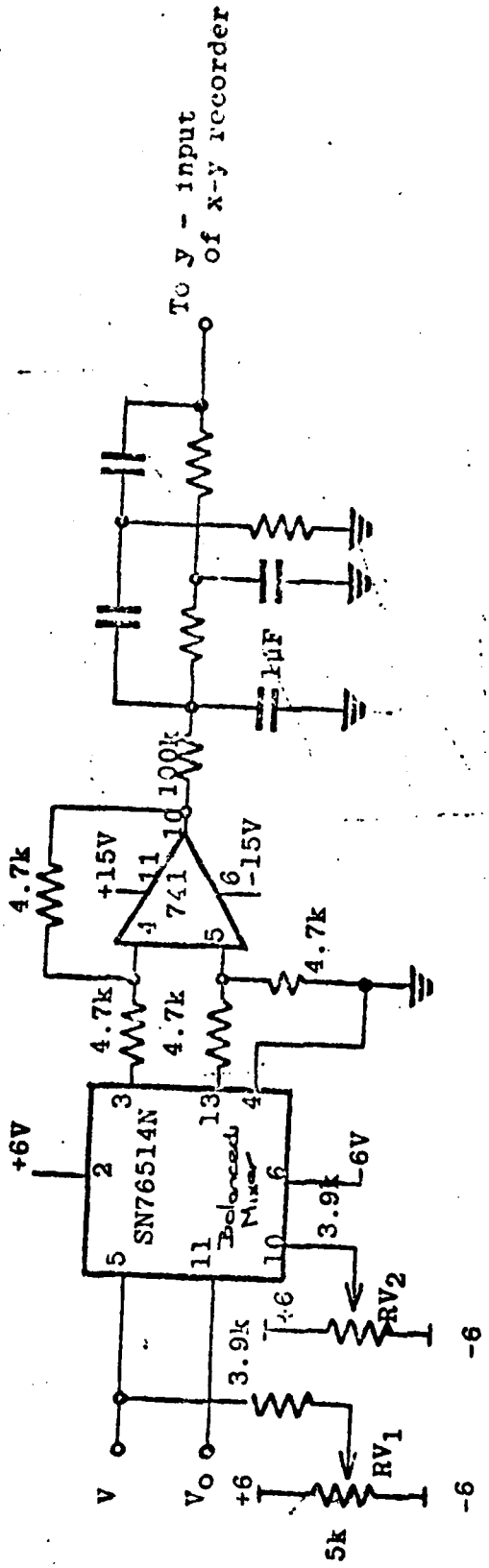

Figure 5

MOS C-V PLOTS BY THE PRESENT PLOTTER AS SUCCESSFULLY EMPLOYED TO STUDY EFFECTS OF ANNEALING ON ANODIC OXIDE OF GaAs

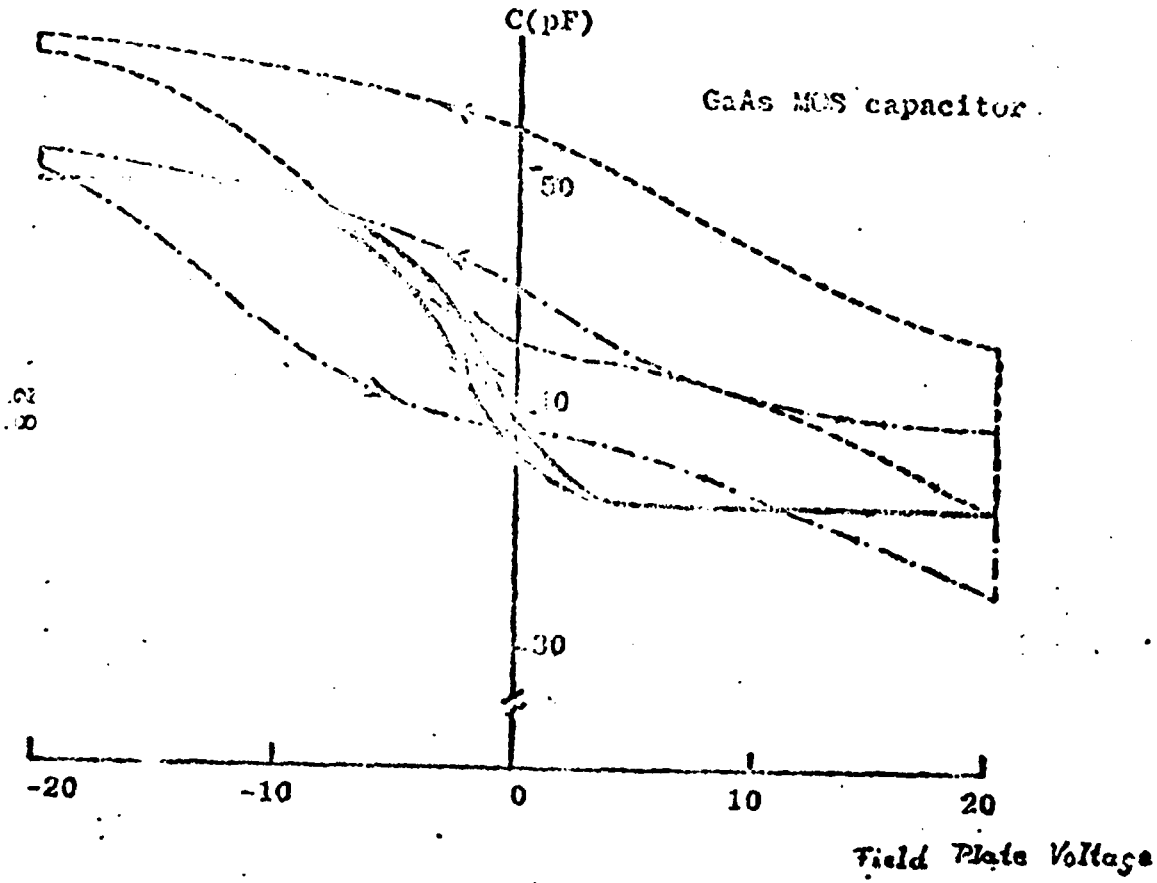

Figure 6(a)

Oxide: anodic native oxide of GaAs
Oxide thickness: 1850 Å
Substrate: (100) p-GaAs, $N_a \simeq 10^{17}$ cm^{-3}
Field plate: Al

	Oxide Condition	Frequency	Ramp Rate
.....	As grown	300 Hz	3 V/S
.....		300 KHz	3 V/S
- - -	Annealed in H2 at 300°C for 1.5 hr	1 MHz	20-400 mV/S

(b) Measurement Conditions

Fig. 6 (b)

APPENDIX II

LIST OF PUBLICATIONS

1. Hartnagel, H., Singh, R., "New Method of Passivating GaAs with Al_2O_3", presented at 1974 International Electron Devices Meeting, Washington D.C., December 1974, Technical Digest p576.

2. Singh, R., Hartnagel, H., "Reduction in Surface Charge Density by New GaAs Passivation Method", accepted for publication in J. Phys. D, Letter.

3. Hasegawa, H., Forward, K.E., Hartnagel, H., "An Improved Method of Anodic Oxidation of GaAs", submitted for publication.

4. Hasegawa, H., Forward, K.E., Hartnagel, H., "New Anodic Native Oxide of GaAs with Improved Dielectric and Interface Properties", submitted for publication.

5. Forward, K.E., Hasegawa, H., Hartnagel, H., "An automatic C-V Plotter", submitted for publication.